1 General Description

The SC32F10T/10G is a series of industrial-grade Flash microcontrollers based on the Arm Cortex-M0+ core, featuring touch functionality. These microcontrollers operate at a high frequency of up to 64MHz. The Cortex-M0+ core utilizes a 32-bit reduced instruction set architecture (RISC) and complies with the CMSIS standard. The SC32F10T/10G series offers powerful data processing capabilities, with an integrated Direct Memory Access (DMA) controller for high-speed data transfer. The hardware CRC module and the built-in 32-bit hardware multiplier further enhance the data computation speed.

The SC32F10T/10G microcontrollers incorporate three clock sources: a high-precision high-frequency 32MHz oscillator (HIRC), a low-frequency 32kHz oscillator (LIRC), and a PLL clock. Additionally, they provide two external crystal oscillator interfaces: a 2-16MHz high-frequency crystal (HXT) interface and a 32.768 KHz low-frequency crystal (LXT) interface. The embedded clock sources and external crystal oscillator interfaces can supply the system clock, and the built-in system clock monitor module switches to HIRC as the clock source in case of system clock abnormalities.

The SC32F10T/10G series offers a wide range of peripheral resources, including a built-in 32-channel high-sensitivity capacitive touch circuit, up to 46 GPIO pins with external interrupt support, 8 16-bit timers, 8 channels of up to 64MHz 16-bit PWM, and 32 channels of 8-bit PWM. It also features 4 independent UARTs, 2 independent SPIs, 2 independent TWIs, built-in LCD/LED hardware drivers, 1 analog comparator, and 13 channels of 14-bit high-precision ADC. The microcontrollers come with an independent watchdog timer (WDT) and a low-voltage reset circuit (LVR) to enhance system reliability. They provide three power modes to meet various power consumption requirements in different application scenarios.

The SC32F10T/10G series delivers high performance and reliability, supporting a wide operating voltage range of 2.0-5.5V and capable of operating in an ambient temperature range of -40°C to 105°C. They also exhibit excellent ESD performance and EFT immunity. In terms of process technology, the SC32F10T/10G series adopts the industry-leading eFlash process, allowing for more than 100,000 write cycles and data retention of 100 years at room temperature. Regarding storage resources, the SC32F10T/10G series offers a maximum of 256 Kbytes of ROM space and 8 Kbytes of SRAM. It includes a built-in system storage area to support OTA upgrades and provides multiple programming methods such as ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application Programming), enabling on-board debugging and firmware updates while the chip is online or powered.

The SC32F10T/10G series excels in touch key (TK) characteristics and possesses outstanding anti-interference performance. It can be adapted to various touch button and master control solutions, finding applications in a wide range of industries including smart appliances, smart homes, the Internet of Things (IoT), wireless communications, gaming consoles, industrial control, and consumer electronics.

2 Features

Operating Conditions

- Operating voltage: 2.0V~5.5V
- Operating temperature: -40 ~ +105℃

EMS

- ESD
  - HBM：MIL-STD-883J Class 3B
  - MM：JEDEC EIA/JESD22-A115 Class C
  - CDM：ANSI/ESDA/JEDEC JS-002-2018 Class C3
- EFT
  - EN61000-4-4 Level 4

Package

- 28 PIN: SOP28 / TSSOP28
- 32 PIN: LQFP32 (7X7) / QFN32 (5X5)
- 44 PIN: LQFP44 (10X10)
- 48 PIN: LQFP48 (7X7) / QFN48 (5X5)

Core

- Cortex®-M0+ core
- With Wakeup Interrupt Controller (WIC) module
- 64-bits instruction prefetch
- Built-in Multiplier Unit (MDU)

Reset

- Power-On Reset (POR)
- Software Reset
- Reset through external NRST pin (PC1) with a low-level signal
- Watchdog Timer (WDT) reset
- Low Voltage Reset (LVR)
  - Four selectable reset voltages: 4.3V, 3.7V, 2.9V, 1.9V
  - The default value is determined by the user's programmed Code Option

BUS

- 1 IOPORT
- 1 AHB
- 3 APB：APB0~APB2

Power Saving Mode

- IDLE Mode，can be woken up by any interrupt
- STOP Mode，can be woken up by INT0~15, Base Timer, TK, and CMP

2.1 Flash

APROM

- Up to 256 Kbytes APROM
- Can be rewritten up to 100,000 times
- Supports hardware read protection encryption
- Supports hardware write protection: Provides two regions for disabling IAP (In-Application Programming) operations. Users can configure the settings through the Code Option, with the minimum setting unit being 512 bytes (one sector)

LDROM

- 2 Kbytes of system storage area, factory-programmed with BootLoader program

SRAM

- 8 Kbytes Internal SRAM
- Supports booting from SRAM

96 bits unique ID

- 96-bit Unique ID defined in the design option area

2.2 BootLoader

- Hardware method: System storage area of 2 Kbytes, factory-programmed with BootLoader program
- Software method: Supports interrupt vector table remapping, allowing flexible partitioning of the APROM area for user BootLoader program execution

2.3 Flash Programming and Emulation

- Programming methods supported: ICP / ISP / IAP
- 2-wire JTAG / SWD programming and emulation interface
- Simulation functionality is not supported in encrypted mode

2.4 Clock source

Built-in high-frequency 32 MHz oscillator (HIRC)

- Can be selected as the system clock source
- Can be selected as the PLL clock source
- Frequency Error: Within ±1% @ -40 ~ 105℃ @ 2.0V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

Built-in low-frequency 32 kHz oscillator (LIRC)

- Can be selected as the system clock source
- Fixed as the WDT clock source, which is always enabled when WDT is enabled
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Frequency Error: Within ±4% @ -20 ~ 85℃ @ 4.0V~ 5.5V, after register correction

External 2~16MHz crystal oscillator (HXT)

- Can be selected as the system clock source
- Can be selected as the PLL clock source
- User can choose an external crystal oscillator oscillating frequency of <12MHz or ≥12MHz

External 32.768 KHz crystal oscillator (LXT)

- Can be selected as the system clock source
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Allows for an external 32.768kHz oscillator
- Automatic calibration of HIRC can be performed using LXT

PLL

- Can be selected as the system clock source
- The PLL clock source can be selected from HIRC or HXT
- The maximum output frequency of PLLRCLK is 64MHz, which can serve as the system clock

2.5 Interrupts (INT)

- Up to 27 interrupts
- Four-level interrupt priority can be set
- External interrupts (INT):
  - 16 interrupts, occupying 4 interrupt vectors in total
  - Change Interrupts on All GPIO pins
  - All interrupts can be set as rising edge, falling edge, or both-edge interrupts, each with an independent corresponding interrupt flag
  - Setting the corresponding interrupt flag in software triggers entry into the corresponding interrupt

2.6 Digtal peripherals

Up to 46 GPIOs

- Independent pull-up resistor configuration is available
- All GPIO pins have source driving capability controlled by four levels
- All GPIO pins have high sink current driving capability (50mA)

Watchdog timer (WDT)

- Built-in WDT with programmable overflow time ranging from 3.94ms to 500ms

Base Timer（BTM）

- The clock sources LXT and LIRC are selectable
- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

8 16-bit timers: Timer0~Timer7

- 16-bit up, down, and up/down auto-reload counters
- Supports rising edge/falling edge capture for PWM duty and period capture
- TIM1~7 can provide individually adjustable PWM (TnPWMA) with controllable duty cycle through the Tn port
- TIM0 can provide individually adjustable PWM (TnPWMB) with controllable duty cycle through the TnEX port
- TIM1/2/6 timer overflow and capture events can trigger DMA requests
- TIM2/3/7 Tn pins support remapping

8 channels 16-bit Advanced PWM0

- The clock source can be selected up to 64MHz
- Shared period and independently adjustable duty cycle
- Support dead time and complementary PWM output
- Support fault detection

32 channels 8-bit LEDPWM

- Shared period and independently adjustable duty cycle
- Support center-aligned mode
- Support fault detection

4 independent UART: UART0~3

- UART2 can be mapped to another set of IO pins
- Independent baud rate generator
- Support wake-up from STOP Mode
- Three communication modes available
  - Mode 0: 8-bit half-duplex synchronous communication
  - Mode 1: 10-bit full-duplex asynchronous communication
  - Mode 3: 11-bit full-duplex asynchronous communication
- UART0 and UART1 support DMA requests
- UART2 and UART3 do not support DMA requests

2 independent SPI: SPI0/SPI1

- SPI0:
  - A 16-bit 8-level FIFO with separate transmit and receive
  - Can be mapped to two additional sets of ports
  - Supports DMA
- SPI1:
  - Can be mapped to another set of ports
  - Supports DMA

2 independent TWI: TWI0/TWI1

- Supports master mode or slave mode
- Supports clock stretching in slave mode
- Communication speed of up to 1Mbps
- TWI0 supports DMA

CRC

- Initial value can be set, with a default of 0xFFFF_FFFF
- Polynomial can be programmed, with a default of 0x04C1_1DB7
- Supports 8/16/32-bit data units

LCD/LED Driver

- The clock sourses LXT and LIRC are selectable
- LCD/LED selection, sharing registers and ports
- LED
  - 8 X 24,6 X 26,5 X 27, or 4 X 28 segment LED drivers
  - LED segment port source drive capability divided into four levels of control
  - Registers shared with 32-channel LEDPWM, enabling LED replacement drive and grayscale adjustment through center-aligned PWM waveforms
- LCD
  - 8 X 24,6 X 26,5 X 27, or 4 X 28 segment LCD drivers
  - Selectable voltage divider resistance for LCD voltage output port
  - Choice of two bias voltages: 1/3 and 1/4
  - Two waveform modes, Type A and Type B, are available
  - Three frame frequencies to choose from:32 Hz to 128 Hz under Type A mode
- The clock sources LXT and LIRC are selectable
- LCD and LED are mutually exclusive options, sharing registers and ports
- LED:
  - Supports 8 X 24, 6 X 26, 5 X 27, or 4 X 28 segment LED driving
  - LED segment port has source driving capability controlled by four levels
  - Shares registers with 32-channel LEDPWM, allowing LED replacement driving and grayscale adjustment through center-aligned PWM waveforms
- LCD:
  - Supports 8 X 24, 6 X 26, 5 X 27, or 4 X 28 segment LCD driving
  - LCD voltage output port has selectable voltage divider resistor values
  - Two bias voltages options: 1/3 and 1/4
  - Two waveform modes: Type A and Type B
  - Three frame frequencies available: 32 Hz to 128 Hz in Type A mode

DMA

- 4 independent configurable channels
- Each DMA channel can send DMA requests to other channels
- Data width supports byte, half-word, and word
- 24 DMA request sources with four priority levels
- Supports source/destination address auto-increment or fixed
- Supports single and burst transfer modes
- Transfer modes: memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral

2.7 Analog peripherals

32-channel high-sensitivity Touch Key circuit

- **Exclusive to the SC32F10T series**
- Channels can be scanned in parallel
- Supports self-capacitance mode and mutual-capacitance mode
- Supports low-power mode
- Supports fast wake-up STOP mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

Analog-to-Digital Converter ADC

- Precison: 14 bits
- Supports up to 13 channels
- External 12 ADC sampling channels can be multiplexed with I/O ports for other functions
- One internal ADC can directly measure VDD voltage
- Four options for ADC reference voltage: VDD, and internal 2.048V, 1.024V, or 2.4V
- Configurable ADC conversion completion interrupt
- Supports single-channel continuous conversion mode
- Supports DMA

Analog Comparator CMP

- Four analog signal positive input terminals: CMP0~CMP3
- Negative input voltage can be selected from CMPR handover or one of the 16 comparison voltages derived from the internal VDD voltage division
- CMP interrupts can wake up the STOP mode

Product Peripheral Resourse Table

Model Peripherals	SC32F10T_ SC32F10G_							
	_C8	_S8	_K8	_G8	_C7	_S7	_K7	_G7
GPIOs	48	44	32	28	48	44	32	28
APROM (Kbyte)	256				128			
SRAM (Kbyte)	8							
TK	SC32F10T_(with TK) & SC32F10G_(without TK)							
SPI	2							
TWI	2							
UART	4							
TIM	8							
PWM0	8	7	5	5	8	7	5	5
LEDPWM	32	29	20	18	32	29	20	18
ADC Channels	12	12	8	6	12	12	8	6
LCD/LED segment	28	26	20	18	28	26	20	18
LCD/LED com	8	7	4	4	8	7	4	4
CRC	YES							
DMA	YES							
Max. CPU frequency	64MHz							

Products naming rules

SC	32	F	1	0	T	C	8	P	J	R

Campany Name
SinOne

Device family
8=8bit
32=32bit

Device type
A=Automotive
F/G=General
L=Ultra-low power
H=High performance
W=Wireless

CPU core
0= Cortex-M0
1= Cortex-M0+

Subseries1
0~9

Subseries2
T=TK
G=GP
M=Motor

Pin count

Label	D	F	E	G	K	T	H	S	C	U	R	J	M	O
Pin count	14	20	24	28	32	36	40	44	48	63	64	72	80	90
Label	V	Q	Z	A	I	B	N	X						
Pin count	100	132	144	169	176	208	216	256						

Flash memory size

Label	0	1	2	3	4	5	6	7	8	9	A	B	C	D
Size（KB）	1	2	4	8	16	32	64	128	256	512	1024	2048	-	-
Label	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Size（KB）	-	-	-	-	-	-	-	72	96	192	384	768	1536	-

Package type

Label	D	M	X	F	T	P	Q	K	S	Y	H	U	W
Package	DIP	SOP	TSSOP	QFP	TQFP	LQFP	QFN	SKDIP	MSOP	WLCSP	BGA	SOT	Wafer

Temperature range
I= -40°C~85°C Industrial
J= -40°C~105°C Automotive G2
A= -40°C~125°C Automotive G1
T= -40°C~150°C Automotive G0

Pack type

R	Tray
T	Tape and Reel
U	Tube
B	Bulk

Ordering Information

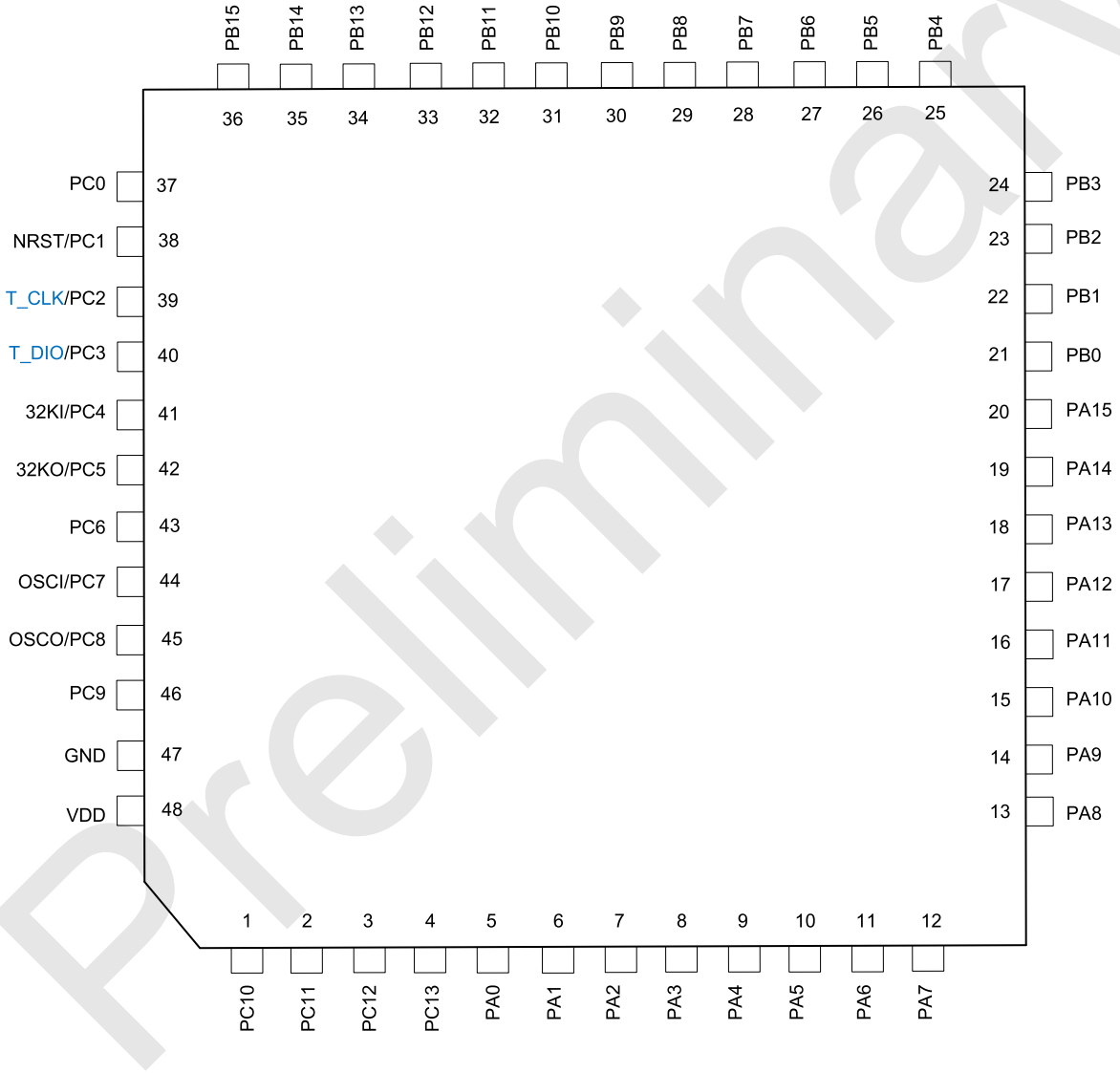
PRODUCT ID	PACKAGE	PACK
SC32F10TC8PJR	LQFP48	TRAY
SC32F10TC8QJR	QFN48	TRAY
SC32F10TS8PJR	LQFP44	TRAY
SC32F10TK8PJR	LQFP32	TRAY
SC32F10TK8QJR	QFN32	TRAY
SC32F10TG8MJU	SOP28	TUBE
SC32F10TG8XJU	TSSOP28	TUBE
SC32F10GC8PJR	LQFP48	TRAY
SC32F10GC8QJR	QFN48	TRAY
SC32F10GS8PJR	LQFP44	TRAY
SC32F10GK8PJR	LQFP32	TRAY
SC32F10GK8QJR	QFN32	TRAY
SC32F10GG8MJU	SOP28	TUBE
SC32F10GG8XJU	TSSOP28	TUBE
SC32F10TC7PJR	LQFP48	TRAY
SC32F10TC7QJR	QFN48	TRAY
SC32F10TS7PJR	LQFP44	TRAY
SC32F10TK7PJR	LQFP32	TRAY
SC32F10TK7QJR	QFN32	TRAY
SC32F10TG7MJU	SOP28	TUBE
SC32F10TG7XJU	TSSOP28	TUBE
SC32F10GC7PJR	LQFP48	TRAY
SC32F10GC7QJR	QFN48	TRAY
SC32F10GS7PJR	LQFP44	TRAY
SC32F10GK7PJR	LQFP32	TRAY
SC32F10GK7QJR	QFN32	TRAY
SC32F10GG7MJU	SOP28	TUBE
SC32F10GG7XJU	TSSOP28	TUBE

Content

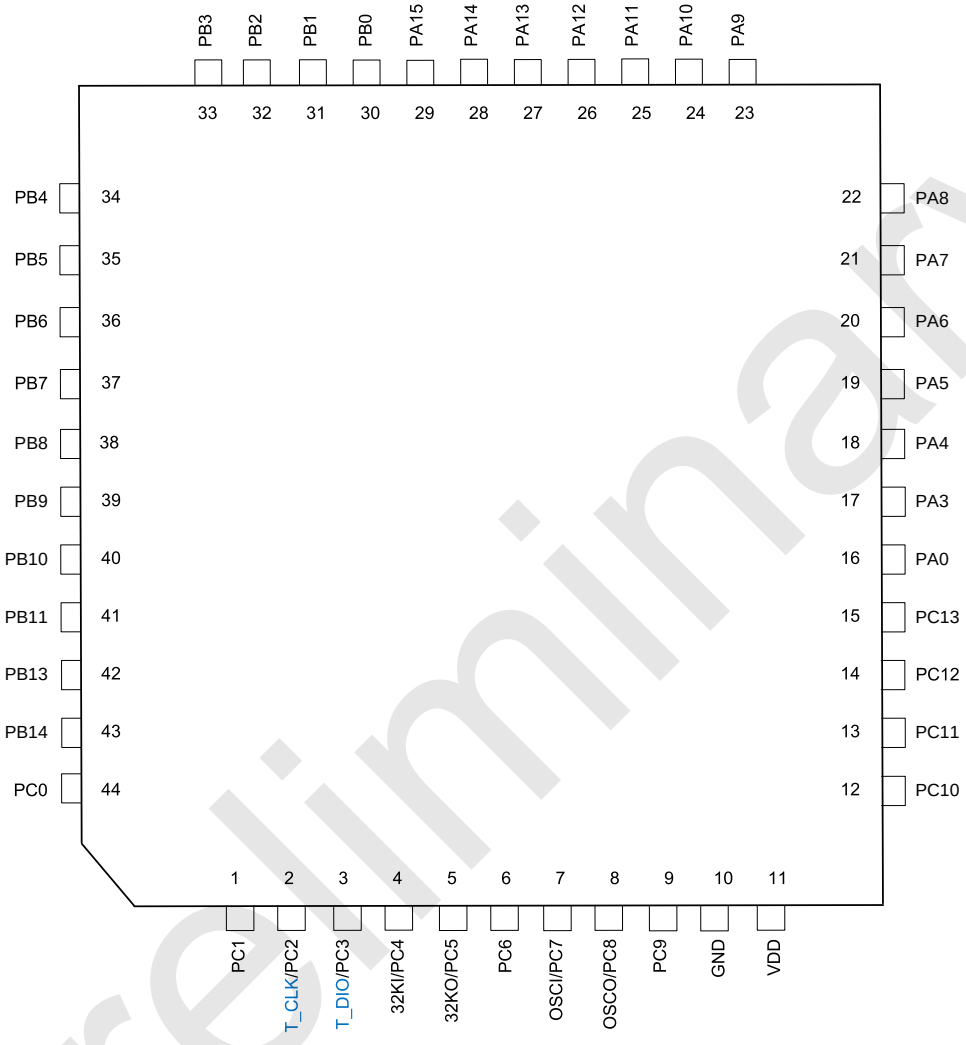
3 Pin Description

3.1 Pin Configuration

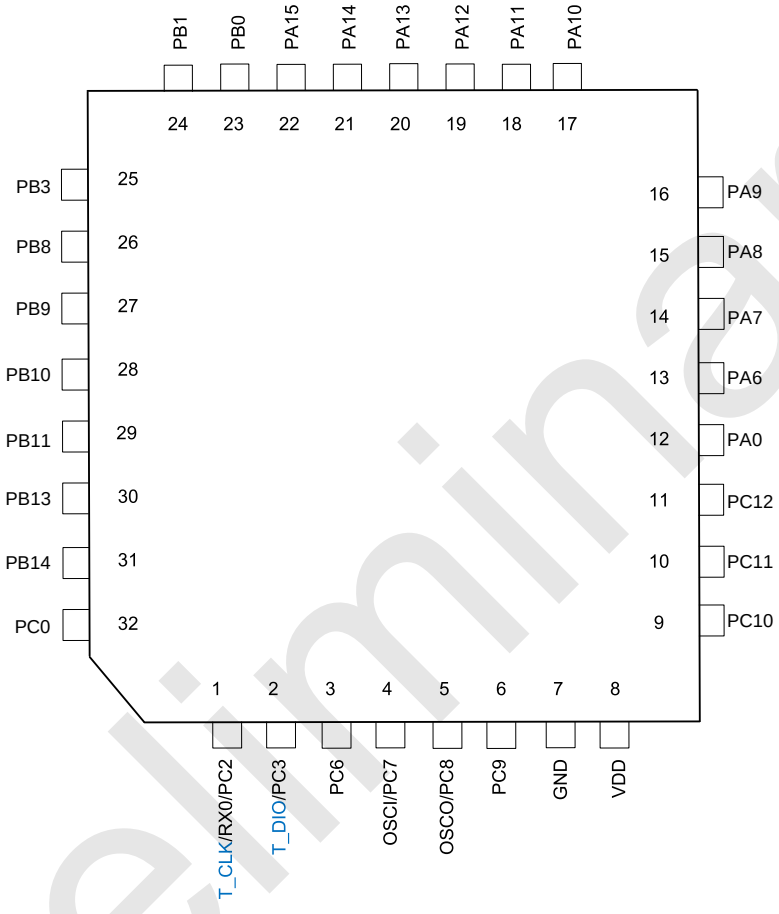
Note： TK function is supported exclusively by the SC32F10T series



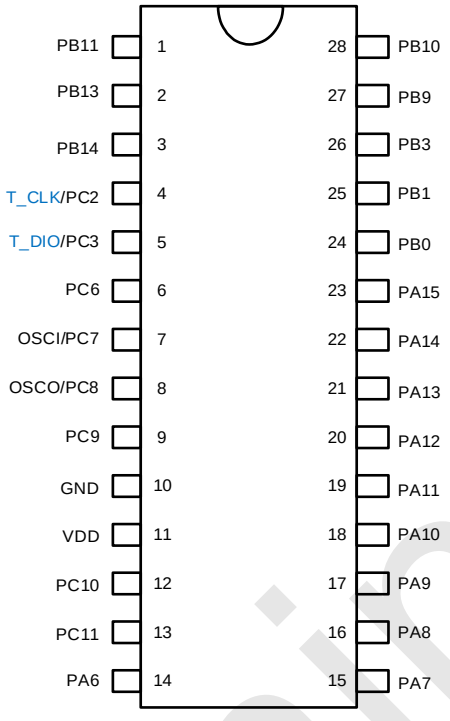
48PIN Pin Diagram
Suitable for LQFP48 & QFN48 package



44PIN Pin Diagram
Suitable for LQFP44 package



32PIN Pin Diagram
Suitable for LQFP32 & QFN32 package



28PIN Pin Diagram
Suitable for SOP28 & TSSOP28 package

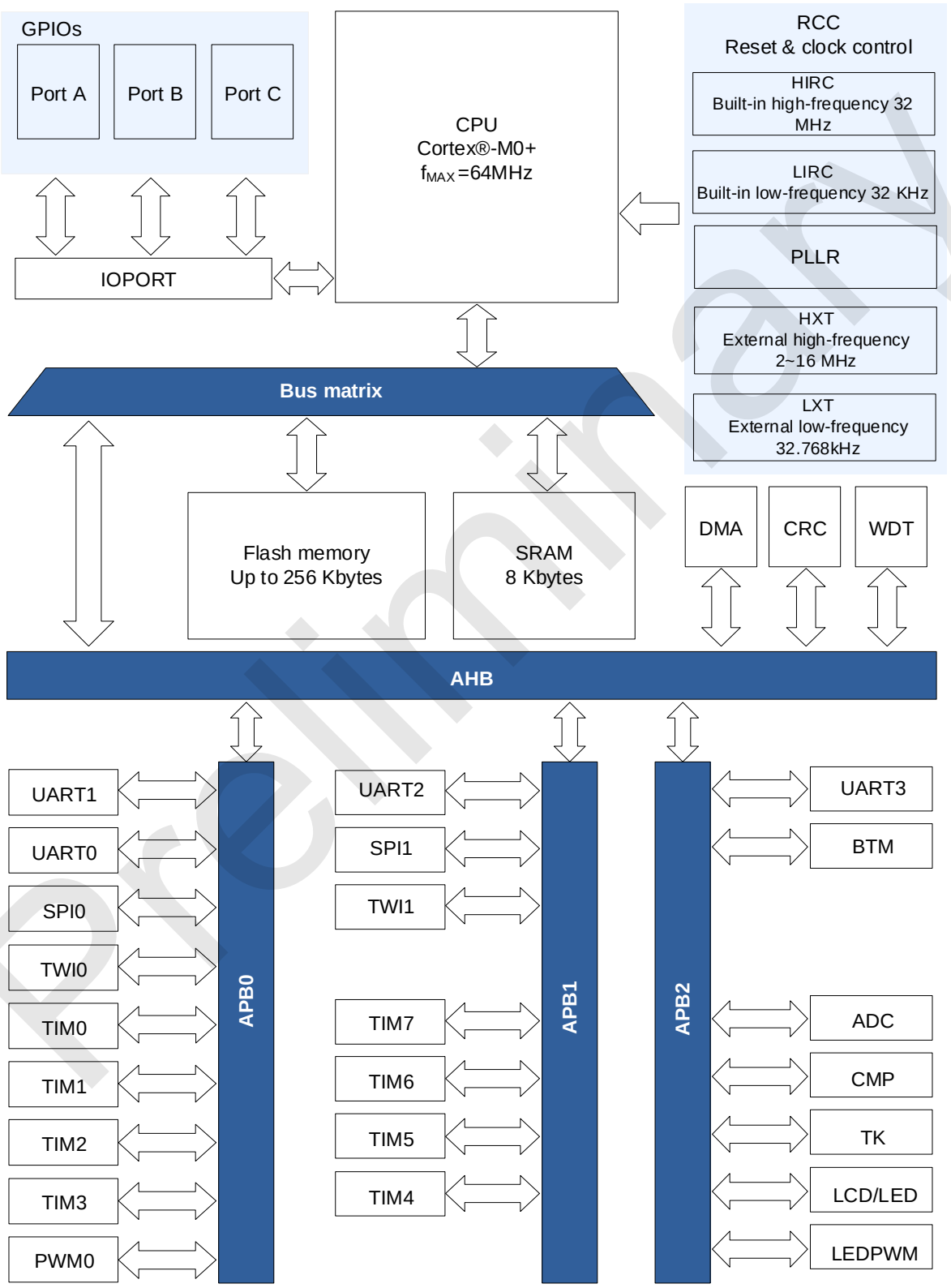
3.2 Pin Resource List

Note: TK function is supported exclusively by the SC32F10T series

LQFP 48	LQFP 44	LQFP 32/QFN32	SOP28/TSSOP 28	Pin Name	Special	TK	LCD/LED	ADC	CMP	PWM-32	PWM-8	UART	SPI	IIC	PWM	TxEX/Tx	INT
1	12	9	12	PC10	-	-	-	-	CMPR	-	-	-	-	SCL0A	-	-	INT10
2	13	10	13	PC11	-	-	-	-	CMP3	-	-	-	-	SDA0A	-	-	INT11
3	14	11	-	PC12	-	TK28	-	-	CMP2	-	-	-	-	-	-	-	INT12
4	15	-	-	PC13	-	TK29	-	-	CMP1	-	-	-	-	-	-	-	INT13
5	16	12	-	PA0	-	TK30	-	-	CMP0	-	-	-	-	-	T3PWMA	T3CAP/T3	INT0
6	-	-	-	PA1	-	TK31	-	-	-	-	-	-	SCK0A	SCL1A	-	-	INT1
7	-	-	-	PA2	-	-	C7	-	-	LEDPWM28	-	-	MOSI0A	SDA1A	-	-	INT2
8	17	-	-	PA3	-	-	C6	-	-	LEDPWM29	PWM4	-	MISO0A	-	-	-	INT3
9	18	-	-	PA4	-	-	C5	-	-	LEDPWM30	PWM5	-	MISO1A	-	-	-	INT4
10	19	-	-	PA5	-	-	C4	-	-	LEDPWM31	PWM6	-	MOSI1A	SDA0B	-	-	INT5
11	20	13	14	PA6	-	TK0	C3/S0	-	-	LEDPWM0	PWM7	-	SCK1A	SCL0B	-	-	INT6
12	21	14	15	PA7	-	TK1	C2/S1	-	-	LEDPWM1	-	-	SCK0B	SCL1B	-	-	INT7
13	22	15	16	PA8	-	TK2	C1/S2	-	-	LEDPWM2	-	-	MOSI0B	SDA1B	-	-	INT8
14	23	16	17	PA9	-	TK3	C0/S3	-	-	LEDPWM3	-	-	MISO0B	-	-	-	INT9
15	24	17	18	PA10	-	TK4	S4	-	-	LEDPWM4	-	TX2A	-	-	T2PWMA	T2CAP/T2	INT10
16	25	18	19	PA11	-	TK5	S5	-	-	LEDPWM5	-	RX2A	-	-	T1PWMA	T1CAP/T1	INT11
17	26	19	20	PA12	-	TK6	S6	-	-	LEDPWM6	-	-	SCK1	SCL1	(T2PWMA)	(T2CAP/T2)	INT12
18	27	20	21	PA13	-	TK7	S7	-	-	LEDPWM7	-	RX1	MOSI1	SDA1/(SCL0C)	(T3PWMA)	(T3CAP/T3)	INT13
19	28	21	22	PA14	-	TK8	S8	-	-	LEDPWM8	-	TX1	MISO1	(SDA0C)	T4PWMA	T4CAP/T4	INT14
20	29	22	23	PA15	-	TK9	S9	-	-	LEDPWM9	-	TX2	MISO0	-	T5PWMA	T5CAP/T5	INT15
21	30	23	24	PB0	-	TK10	S10	-	-	LEDPWM10	-	RX2	MOSI0	SDA0	T6PWMA	T6CAP/T6	INT0
22	31	24	25	PB1	-	TK11	S11	-	-	LEDPWM11	FLT	-	SCK0	SCL0	(T7PWMA)	(T7CAP/T7)	INT1
23	32	-	-	PB2	-	TK12	S12	-	-	LEDPWM12	-	-	-	-	-	-	INT2
24	33	25	26	PB3	-	TK13	S13	AIN7	-	LEDPWM13	-	-	-	-	-	-	INT3
25	34	-	-	PB4	-	TK14	S14	AIN8	-	LEDPWM14	-	-	-	-	-	-	INT4

LQFP 48	LQFP 44	LQFP 32/QFN32	SOP28/TSSOP 28	Pin Name	Special	TK	LCD/LED	ADC	CMP	PWM-32	PWM-8	UART	SPI	IIC	PWM	TxEX/Tx	INT
26	35	-	-	PB5	-	TK15	S15	AIN9	-	LEDPWM15	-	-	-	-	-	-	INT5
27	36	-	-	PB6	-	TK16	S16	AIN10	-	LEDPWM16	-	-	-	-	-	-	INT6
28	37	-	-	PB7	-	TK17	S17	AIN11	-	LEDPWM17	-	-	-	-	-	-	INT7
29	38	26	-	PB8	-	TK18	S18	AIN12	-	LEDPWM18	-	-	-	-	-	-	INT8
30	39	27	27	PB9	-	TK19	S19	AIN13	-	LEDPWM19	-	-	-	-	-	-	INT9
31	40	28	28	PB10	-	TK20	S20	AIN14	-	LEDPWM20	-	-	-	-	-	-	INT10
32	41	29	1	PB11	-	TK21	S21	AIN15	-	LEDPWM21	-	-	-	-	-	-	INT11
33	-	-	-	PB12	-	TK22	S22	-	-	LEDPWM22	-	-	-	-	-	-	INT12
34	42	30	2	PB13	-	TK23	S23	-	-	LEDPWM23	-	RX3	-	-	-	-	INT13
35	43	31	3	PB14	-	TK24	S24	-	-	LEDPWM24	-	TX3	-	-	-	-	INT14
36	-	-	-	PB15	-	TK25	S25	-	-	LEDPWM25	-	-	-	-	T0PWMB	T0EX	INT15
37	44	32	-	PC0	-	TK26	S26	AIN16	-	LEDPWM26	-	-	-	-	-	-	INT0
38	1	-	-	PC1	NRST	TK27	S27	-	-	LEDPWM27	-	-	-	-	T7PWMA	T7CAP/T7	INT1
39	2	1	4	PC2	T_CLK	-	-	-	-	-	-	RX0	-	-	-	-	INT2
40	3	2	5	PC3	T_DIO	-	-	-	-	-	-	TX0	-	-	-	-	INT3
41	4	-	-	PC4	32KI	-	-	-	-	-	-	-	-	-	-	-	INT4
42	5	-	-	PC5	32KO	-	-	-	-	-	-	-	-	-	-	-	INT5
43	6	3	6	PC6	-	-	-	AIN0	-	-	PWM3	-	-	-	-	-	INT6
44	7	4	7	PC7	OSCI	-	-	-	-	-	PWM2	-	-	-	-	-	INT7
45	8	5	8	PC8	OSCO	-	-	-	-	-	PWM1	-	-	-	-	-	INT8
46	9	6	9	PC9	-	Cmod	-	AIN1	-	-	PWM0	-	-	-	-	-	INT9
47	10	7	10	GND	Power	-	-	-	-	-	-	-	-	-	-	-	-
48	11	8	11	VDD	Power	-	-	-	-	-	-	-	-	-	-	-	-

4 Resource Diagram



5 Power,Reset And System Clock（RCC）

5.1 Power-on Reset

After the SC32F10T/10G power-on, the processes carried out before execution of client software are as follows:

- Reset stage
- Loading information stage
- Normal operation stage

5.1.1 Reset Stage

The SC32F10T/10G will always be reset until the voltage supplied to SC32F10T/10G is higher than a certain voltage, and the internal Clock starts to be effective. The duration of reset stage is related to rising speed of external power. Once the external supply voltage is up to built-in POR voltage, the reset stage would be completed.

5.1.2 Loading Information Stage

There is a warm-up counter inside The SC32F10T/10G. During the reset stage, the warm-up counter is cleared to 0 until the voltage exceeds the POR voltage, the built-in HIRC oscillator starts to oscillate, and the warm-up counter starts counting. When the internal warm-up counter counts to a certain number, every certain number of HIRC clocks will read a byte of data from the IFB (including Customer Option) in the Flash ROM and store it in the internal system register. This reset signal will not end until the warm-up is completed.

5.1.3 Normal Operation Stage

After finishing the Loading Information stage, The SC32F10T/10G starts to read the instruction code from Flash and enters the normal operation stage. The LVR voltage is the set value of Customer Option written by the user.

5.2 Reset Modes

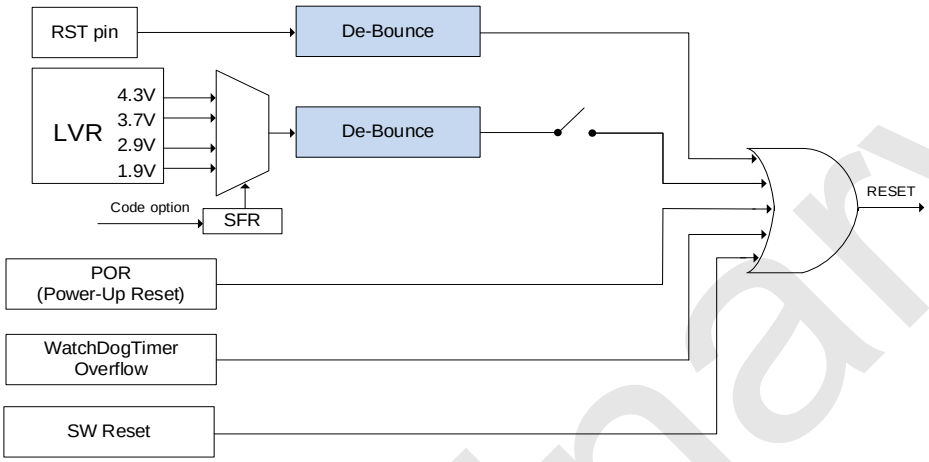
The SC32F10T/10G has 5 reset methods, the first four are hardware reset:

1. External reset
2. Low-voltage reset LVR
3. Power-on reset POR

4. Watchdog WDT reset

5. Software reset.

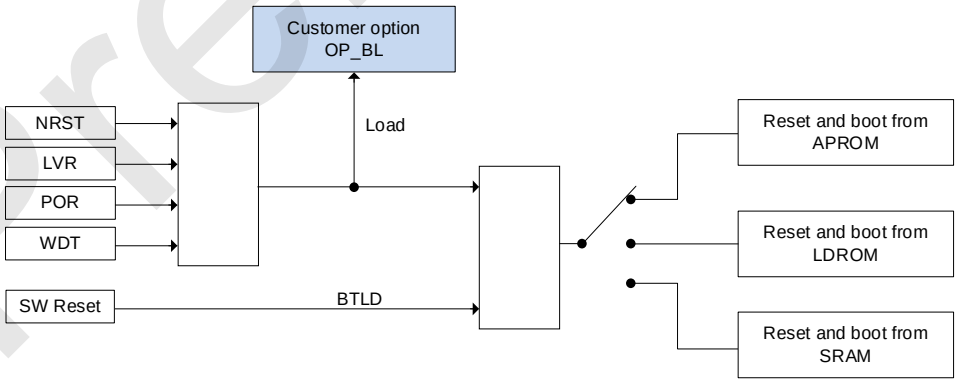
The circuit diagram of the reset part of the SC32F10T/10G is as follows:



SC32F10T/10G Reset Circuit Diagram

5.2.1 Boot area after the reset

After hardware reset through external RST, low voltage reset (LVR), power-on reset (POR), or watchdog reset (WDT), the chip boots from the startup area (APROM / LDROM / SRAM) set by the user in OP_BL. After the software reset, the chip boots from the startup area (APROM / LDROM / SRAM) set by BTLD[1:0].



SC32F10T/10G Boot Area Switching diagram after reset

5.2.2 External RST

External reset is a low-level reset pulse signal of a certain width given to SC32F10T/10G from external RST pin to realize the reset of SC32F10T/10G. User can configure the PC1/NRST pin as RST (reset pin) using the programming host software by Customer Option before programming.

5.2.3 Low-voltage Reset LVR

The SC32F10T/10G provides a low-voltage reset circuit. There are 4-level LVR voltage options: 4.3V, 3.7V, 2.9V, 1.9V. The default value is the Customer Option value written by the user. A reset occurs when the VDD voltage is less than the threshold voltage for low-voltage reset and the duration is greater than T_{LVR}. Among them, T_{LVR} is the buffeting time of LVR, about 30μs.

5.2.4 Power-on Reset(POR)

The SC32F10T/10G has a power-on reset circuit inside. When the power supply voltage V_{DD} reaches the POR reset voltage, the system automatically resets.

5.2.5 Watchdog Reset(WDT)

The SC32F10T/10G has a WDT, the clock source of which is the built-in 32 kHz oscillator. The user can choose whether to enable the watchdog reset function by Customer Option.

5.2.6 Software Reset

Enable RST(IAP_CON.8) will immediately reset the system.

5.2.7 Initial Reset State

When SC32F10T/10G is in the reset state, most registers return to their initial state. The watchdog (WDT) is in the disabled state. 'Hot-start' resets (such as WDT, LVR, software reset, etc.) do not affect SRAM, and SRAM values remain the same as before the reset. Loss of SRAM content occurs when the power supply voltage drops to a level where RAM cannot retain data.

5.3 Clock

5.3.1 System Clock Source

Five different clock sources can be used to drive the system clock (SYSCLK):

- Built-in high-frequency 32MHz oscillator (HIRC), default clock at power-up
- External high-frequency crystal oscillator (HXT)
- Built-in low-frequency 32KHz oscillator (LIRC)
- External low-frequency crystal oscillator (LXT)
- PLL, with a maximum frequency of 64MHz

Note：

1. The default system clock source at power-up is HIRC. Users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.

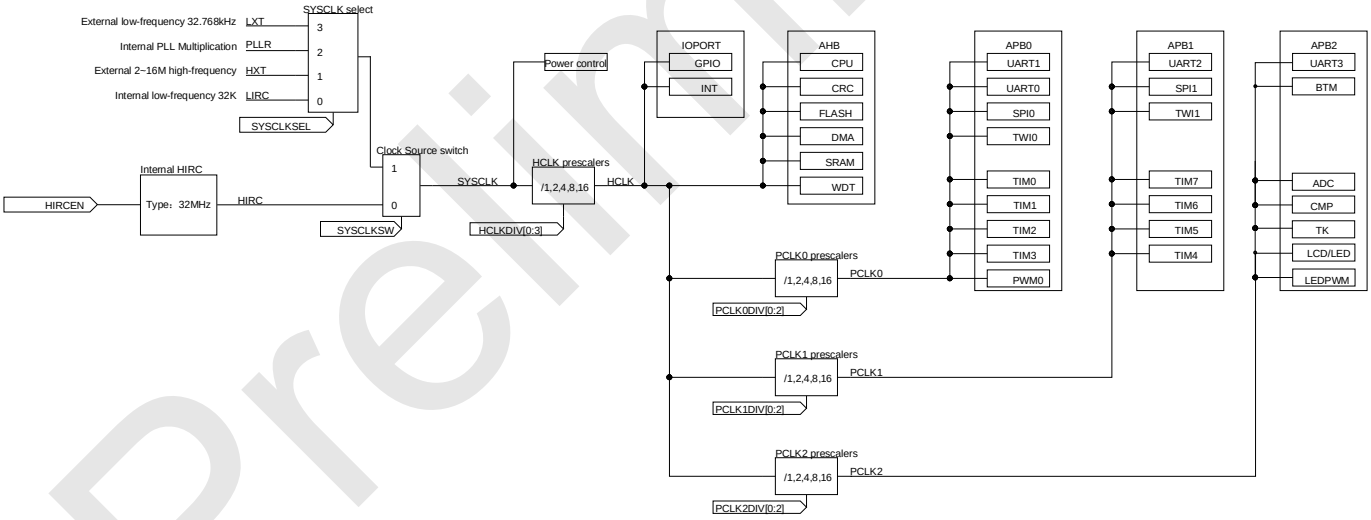
2. Regardless of the chosen clock source to switch to, the system clock source must first be switched to HIRC before transitioning to the target clock source.

5.3.2 Bus

- Users can configure the frequencies of the AHB, APB0, APB1, and APB2 domains through multiple prescalers. HCLK: The main clock of the AHB domain, with a maximum frequency of 64MHz. It drives components such as the Cortex®-M0+ core, memory, and DMA.
- PCLK0: The main clock of the APB0 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB0 bus are driven by PCLK0.
- PCLK1: The main clock of the APB1 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB1 bus are driven by PCLK1.
- PCLK2: The main clock of the APB2 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB2 bus are driven by PCLK2.

The RCC divides the AHB clock (HCLK) by 8 to serve as the external clock for SysTick. By setting the control and status registers of SysTick, you can choose either the above-mentioned clock or the core clock as the SysTick clock source.

5.3.3 Clock and Bus Allocation Block Diagram



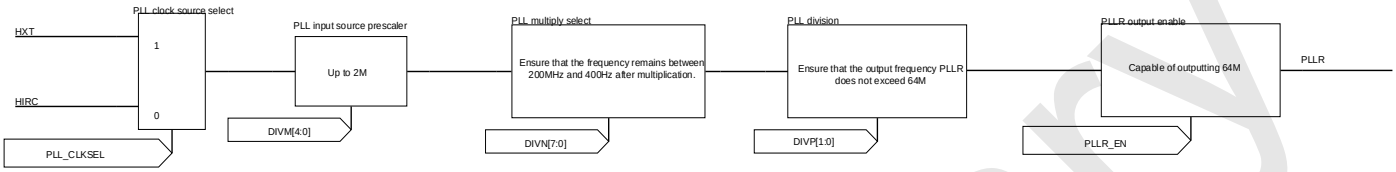
Clock and Bus Allocation Block Diagram

5.4 RCC Interrupt

In coordination with the stop oscillation detection mechanism, SC32F10T/10G's clock source provides a user-configurable RCC interrupt: when the system clock source is LXT/HXT/PLL, if an abnormality is detected in the clock source, the stop oscillation detection interrupt flag will be set. If the corresponding interrupt is enabled at this point, a stop oscillation detection interrupt will be generated.

5.5 PLL

- The system operating clock can be multiplied to 64MHz through PLL.
- Users can configure the desired frequency using the formula:
  - PLL input clock frequency f_{PLL_IN}
  - PLL output frequency f_{PLLR} = [(f_{PLL_IN} / DIVM) * DIVN] / 2 ^ (DIVP +1)
- The PLL circuit diagram is as follows:



5.6 Built-in high-frequency 32MHz oscillator (HIRC)

- Can be selected as the system operating clock
- Can be selected as the PLL clock source
- Frequency error: Within ±1% @ -40 ~ 105℃ @ 2.0V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

5.7 External High-Frequency Crystal Oscillator Circuit (HXT)

- Can be selected as the system operating clock
- Can be selected as the PLL clock source
- Can be externally connected to a 2~16MHz high-frequency oscillator

5.8 Built-in Low-Frequency 32kHz Oscillator

- Can be selected as the system operating clock
- Can be selected as the LCD/LED clock source
- Can be selected as the Base Timer and WDT clock source
- Frequency error: Within ±4% @ -20 ~ 85℃ @ 4.0V~ 5.5V, after register correction

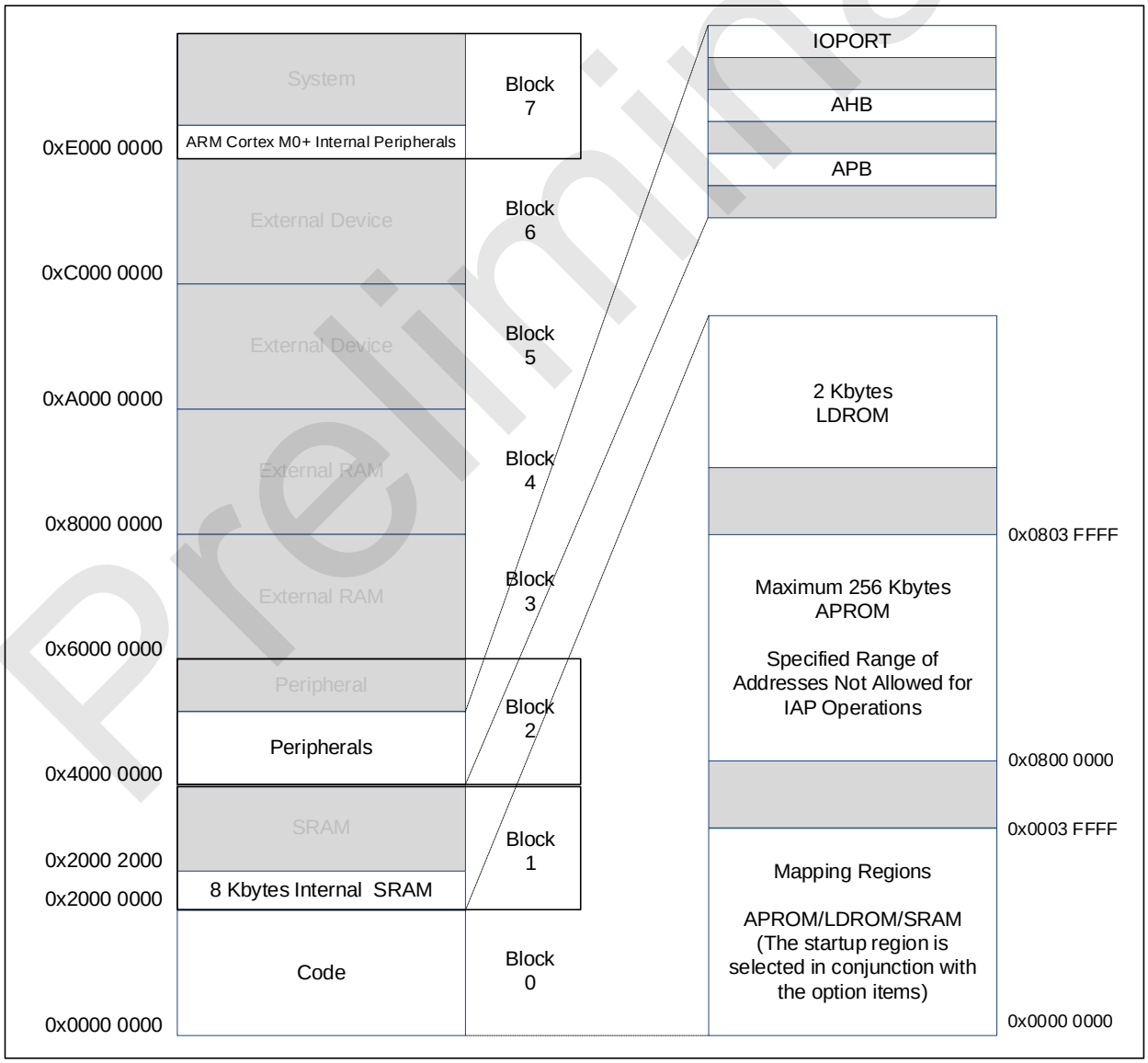
5.9 External Low-Frequency Oscillator Circuit (LXT)

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Allows for an external 32.768kHz low-frequency oscillator
- Automatic calibration of HIRC can be performed using LXT

6 Flash

- The Flash width is 32 bits, and it can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature
- The structure of the Flash includes:
  - Maximum 256 Kbytes APROM
  - 2 Kbytes LDROM
  - 8 Kbytes Internal SRAM
  - 96 bits Unique ID

6.1 Storage Block Diagram



SC32F10T/10G Series Memory Mapping Diagram

6.2 APROM

- APROM of SC32F10xx8 series has 256Kbytes
- APROM of SC32F10xx7 series has 128Kbytes
- Sector Size: 512 bytes
- Supports: Read/Write/Sector Erase/Chip Erase/Blank Check
- The CPU (Cortex®-M0+) accesses Flash through the AHB bus
- The program defaults to booting from APROM, and users can select programs to boot from other areas such as SRAM/LDROM using the customer option OP_BL[1:0].
- Read Protection: After enabling read protection, only a program that runs from APROM can read information from APROM. Other areas or third-party tools cannot access information from APROM.
- Write Protection: Provides two hardware read protection regions where IAP operations are prohibited. Users can set the range of the two read protection regions in units of sectors based on actual needs.

The 256 Kbytes of APROM is divided into 512 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer before writing data. During user write operations, the sector must be erased first before writing data.

SC32F10xx8serise 256 Kbytes APROM Sector Partition Illustration

128 Kbytes of APROM is divided into 256 sectors, with each sector being 512 bytes. During programming, the sector corresponding to the target address is forcibly erased by the programmer before writing data. For user write operations, erasure must precede data writing.

SC32F10xx7series 128 Kbytes APROM Sector Partition Illustration

6.3 LDROM

- 2 Kbytes of system storage area, factory-programmed with BootLoader program, Users cannot modify or access this area.
- Embedded Bootloader Program: The fixed ISP program is publicly available, allowing reprogramming of Flash via UART. The program waits for upgrade commands, and if no update command is received within 500 milliseconds, it jumps to APROM for execution (0X8000 0000).

6.3.1 BootLoader

Supports two Bootloader modes:

- Software Approach: Directly partition BootLoader and APP areas in software. Easy sharing interrupts of BootLoader and APP by modifying VTOR. Flexible adjustment of the size of each area；
- Hardware Approach: 2 Kbytes fixed "LDROM" as a dedicated BootLoader area that users cannot read or write
  - LDROM serves as a fixed BootLoader space with factory-programmed program, and users cannot read or write
  - Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

6.4 SRAM

- Internal SRAM：8 Kbytes，address 0x2000 0000 ~ 0x2000 1FFF
- Users can choose to start the program from SRAM by configuring the customer option OP_BL[1:0].
- It supports byte, half-word (16-bit), or word (32-bit) access at the maximum system clock frequency, with no waiting states. Therefore, it can be accessed by both the CPU and DMA

6.5 Boot Area Selection (Bootstrap)

After a reset, users can independently configure the desired bootstrap mode.

After exiting the standby mode, the startup mode configuration can be resampled. Once this startup delay has ended, the CPU will fetch the stack top value from address 0x00000000 and then begin executing code from the bootstrap memory starting at 0x00000004.

There are three options for bootstrap area selection: Main Flash Memory Area, System Flash Memory Area and SRAM, described in detail as follows:

6.5.1 Bootstrap from APROM

APROM is aliased in the bootstrap memory space (0x00000000) but can also be accessed from its original memory space (0x08000000). In other words, the program can start accessing from either address 0x00000000 or 0x08000000.

6.5.2 Bootstrap from LDROM

- 2 Kbytes LDROM serves as a fixed BootLoader space with factory-programmed program, Users cannot modify or access this area.
- Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

6.5.3 Bootstrap from SRAM

SRAM has an alias in the bootstrap memory space (0x0000 0000) but can also be accessed from its original memory space (0x2000 0000).

6.5.4 Bootstrap mode config

The bootstrap modes can be controlled by the register bits BTLD[1:0] in conjunction with the software reset (RST) control bit, both protected by the IAP_KEY:：

① Set BTLD[1:0]=0x00: the chip boots from APROM after a software reset

② Set BTLD[1:0]=0x01: the chip boots from LDROM after a software reset

③ Set BTLD[1:0]=0x10: the chip boots from SRAM after a software reset

The initial boot region selection during power-up can be configured by customer option bits OP_BL[1:0]:

① Set OP_BL[1:0]=0x00: the chip boots from APROM after a software reset

② Set OP_BL[1:0]=0x01: the chip boots from LDROM after a software reset

③ Set OP_BL[1:0]=0x10: the chip boots from SRAM after a software reset

6.6 96 bits Unique ID

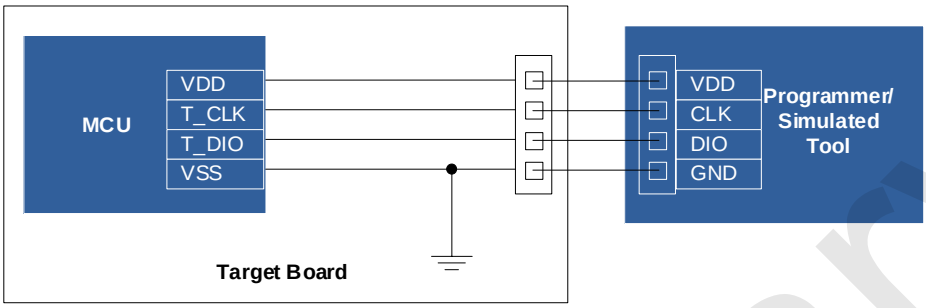
The SC32F10T/10G provides an independent Unique ID area. A 96-bit unique code can be pre-programmed before leaving the factory to ensure the uniqueness of the chip. The only way for the user to obtain the serial number is to read through the IAP instruction.

6.7 User ID Area

User ID area, where user-costomized ID is pre-programmed when leaving the factory. Users can read the User ID area, but cannot write the User ID area.

6.8 Programming

The SC32F10T/10G's Flash can be programmed through T_DIO, T_CLK, VDD, VSS, the specific connection relationship is as follows:



ICP mode Flash Writer programming connection diagram

T_DIO、T_CLK is a 2-wire JTAG programming and emulation signal line. Users can configure the mode of these two ports through the Customer Option when programming.

6.8.1 JTAG Specific Mode

T_DIO,T_CLK are specific port for programming and emulation, and other functions multiplexed with it are not available.

This mode is generally used in the online debugging stage, which is convenient for users to simulate and debug. After the JTAG special mode takes effect, the chip can directly enter the programming or emulation mode without powering on and off again.

6.8.2 Normal Mode (JTAG specific port is invalid)

The JTAG function is not available, and other functions multiplexed with it can be used normally. This mode can prevent the programming port from occupying the MCU pins, which is convenient for users to maximize the use of MCU resources.

Note: When the invalid configuration setting of the JTAG dedicated port is successful, the chip must be completely powered off and then on again to enter the programming or emulation mode, which will affect the programming and emulation in the live mode. SinOne recommends that users select the invalid configuration of the JTAG dedicated port during mass production and programming, and select the JTAG mode during the development and debugging phase.

6.9 Security Encryption

- The SC32F10T/10G series mainly involves encrypting the APROM for read protection. Users can configure the read protection encryption feature during programming through the customer option in the dedicated programming

host; enable flash read protection can enter encryption mode: The chip defaults to a non-encrypted state while leaving the factory

- The read protection encryption feature has no mapped registers. Users can only modify it after config the customer option in the dedicated programming host and programming.
- Encryption Disabled: Operations such as reading, programming, and erasing can be performed on APROM. These operations can be also performed on Bytes and backup registers.
- Encryption Enabled:
  - Enable from APROM: Code executed in user mode (booting from user APROM) can perform all operations on APROM.
  - Debug, enable from SRAM and LDROM: In debug mode or when code is booted from SRAM or LDROM, APROM is completely inaccessible.
- Disabling encryption requires a full erase operation on APROM.

6.9.1 Security Encryption Access Rights

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Earse	Full Earse	Operate Write-Protection Region	Read	Write	Block Earse	Full Earse	Operate Write-Protection Region
Bootstrap from APROM	√	√	√	\	Forbid	√	√	√	\	Forbid
Debug/Bootstrap from SRAM	√	√	√	√	Forbid	Forbid	Forbid	Forbid	Forbid	Forbid
Bootstrap from LDROM	√	√	√	√	√	Forbid	Forbid	Forbid	√	Forbid

6.10 In Application Programming (IAP)

The IAP (In Application Programming) area in the APROM of SC32F10T/10G allows users to perform remote program updates through IAP operations. Users can also retrieve information from the Unique ID or User ID areas by IAP read operations. Before performing IAP write operations, users must carry out sector erasure for the target address sector.

The chip allows global IAP operations in the APROM by default while leaving the factory. Internally, the chip provides two sets of flash write protection regions. These regions are set based on sector units, and the protected areas are restricted from IAP operations. The rules for setting these regions are as follows:

IAPPORx Register Value（x=A or B）	IAPPOR Protection Area
IAPPORx_ST = IAPPORx_ED	Sector IAPPORx
IAPPORx_ST > IAPPORx_ED	No protection
IAPPORx_ST < IAPPORx_ED	Sectors from IAPPORx_ST to IAPPORx_ED

User can config these APROM's write protection area through "Customer Option" while programming.

7 Interrupts

- M0+ core could provide a maximum of 32 interrupt sources, numbered from 0 to 31, while SC32F10T/10G series has 27 interrupt sources.
- Four-level interrupt priorities can be configured, and the interrupt priorities are set through the Interrupt Priority Registers in the core registers.

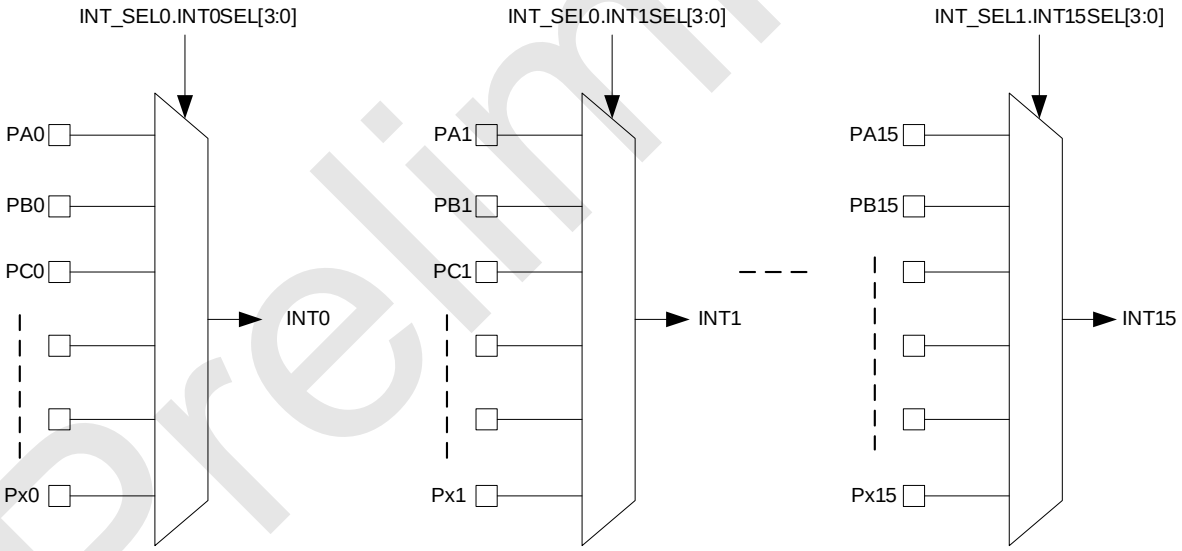
7.1 External interrupts INT0~15

External interrupts comprise 16 interrupt sources, occupying a total of 4 interrupt vectors. All 16 external interrupt sources can be configured to respond to rising edges, falling edges, or both edges. Once configured, these interrupts can cover all GPIO pins. When the corresponding event occurs, software sets the corresponding interrupt flag (RIF/FIF to 1), triggering entry into the corresponding interrupt service.

The external interrupt features of the SC32F10T/10G series are as follows:

- 16 INT interrupt sources, occupying 4 interrupt vectors in total.
- After configuration, INT can cover all GPIO pins.
- All INT sources can be configured for rising edge, falling edge, or both edge interrupts, each having independent corresponding interrupt flag.

Note: When using INT functions, users need to manually set the GPIO port corresponding to INTn (n=0~15) to pull-up input mode. External interrupts cannot be detected in output mode.



External Interrupt Port Multiplexer

7.2 Interrupt and Events

- When NVIC is disabled, interrupt request masks are enabled, events can be generated, but interrupt cannot be generated.
- When NVIC is enabled, interrupt request masks act as internal master interrupt control bit in the module.

7.3 Interrupt Source and Vector

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
0	-	-	0x0000_0000	-		-	\	\	YES
1	-	Fixed	0x0000_0004	RESET	PRIMASK	SCB	\	\	YES
2	-	Fixed	0x0000_0008	NMI_Handler		SCB	\	\	YES
3	-	Fixed	0x0000_000C	HardFault_Handler	PRIMASK	SCB	\	\	YES
4~10	-	-	0x0000_0010 - 0x0000_0028	-		-	\	\	YES
11	-	Settable		SVC_Handler	PRIMASK	SCB	\	\	YES
12~13	-	-	0x0000_0030 0x0000_0034	-		-	\	\	YES
14	-	Settable	0x0000_0038	PendSV_Handler	PRIMASK	SCB	\	\	YES
15	-	Settable	0x0000_003C	SysTick_Handler	PRIMASK	SysTick_CTRL	\	\	YES
16	0	Settable	0x0000_0040	INT0	NVIC->ISER[0].0	INTF_IE->ENFx，x=0 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
17	1	Settable	0x0000_0044	INT1-7	NVIC->ISER[0].1	INTF_IE->ENFx，x=1~7 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
18	2	Settable	0x0000_0048	INT8-11	NVIC->ISER[0].2	INTF_IE->ENFx，x=8~11 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
19	3	Settable	0x0000_004C	INT12-15	NVIC->ISER[0].3	INTF_IE->ENFx，x=12~15 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
20	4	Settable	0x0000_0050	RCC 停振检测	NVIC->ISER[0].4	RCC_CFG->INTEN	\	RCC_STS->CLKFIF	YES
21	5	Reserved	0x0000_0054	\	\	\	\	\	
22	6	Settable	0x0000_0058	BTM	NVIC->ISER[0].6	BTM_CON->INTEN	\	BTM_STS->BTMIF	YES
23	7	Settable	0x0000_005C	UART0	NVIC->ISER[0].7	UART0_IDE->INTEN	UART0_IDE->TXIE UART0_IDE->RXIE	UART0_STS->TXIF UART0_STS->RXIF	NO
				UART2	\	UART2_IDE->INTEN	UART2_IDE->TXIE UART2_IDE->RXIE	UART2_STS->TXIF UART2_STS->RXIF	
24	8	Settable	0x0000_0060	UART1	NVIC->ISER[0].8	UART1_IDE->INTEN	UART1_IDE->TXIE UART1_IDE->RXIE	UART1_STS->TXIF UART1_STS->RXIF	NO

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
				UART3	\	UART3_IDE->INTEN	UART3_IDE->TXIE UART3_IDE->RXIE	UART3_STS->TXIF UART3_STS->RXIF	
25	9	Settable	0x0000_0064	SPI0	NVIC->ISER[0].9	SPI0_IDE->INTEN	SPI0_IDE->RXNEIE SPI0_IDE->TBIE SPI0_IDE->RXIE SPI0_IDE->RXHIE SPI0_IDE->TXHIE	SPI0_STS->SPIF SPI0_STS->RXNEIF SPI0_STS->TXEIF SPI0_STS->RXFIF SPI0_STS->RXHIF SPI0_STS->TXHIF	NO
26	10	Settable	0x0000_0068	SPI1	NVIC->ISER[0].10	SPI1_IDE->INTEN	\	SPI1_STS->TXHIF	NO
27	11	Settable	0x0000_006C	DMA0	NVIC->ISER[0].11	DMA0_CFG->INTEN	DMA0_CFG->TCIE DMA0_CFG->HTIE DMA0_CFG->TEIE	DMA0_STS->GIF DMA0_STS->TCIF DMA0_STS->HTIF DMA0_STS->TEIF	NO
28	12	Settable	0x0000_0070	DMA1	NVIC->ISER[0].12	DMA1_CFG->INTEN	DMA1_CFG->TCIE DMA1_CFG->HTIE DMA1_CFG->TEIE	DMA1_STS->GIF DMA1_STS->TCIF DMA1_STS->HTIF DMA1_STS->TEIF	NO
29	13	Settable	0x0000_0074	DMA2	NVIC->ISER[0].13	DMA2_CFG->INTEN	DMA2_CFG->TCIE DMA2_CFG->HTIE DMA2_CFG->TEIE	DMA2_STS->GIF DMA2_STS->TCIF DMA2_STS->HTIF DMA2_STS->TEIF	NO
30	14	Settable	0x0000_0078	DMA3	NVIC->ISER[0].14	DMA3_CFG->INTEN	DMA3_CFG->TCIE DMA3_CFG->HTIE DMA3_CFG->TEIE	DMA3_STS->GIF DMA3_STS->TCIF DMA3_STS->HTIF DMA3_STS->TEIF	NO
31	15	Settable	0x0000_007C	TIM0	NVIC->ISER[0].15	TIM0_IDE->INTEN	TIM0_IDE->TIE TIM0_IDE->EXFIE TIM0_IDE->EXRIE	TIM0_STS->TIF TIM0_STS->EXIF TIM0_STS->EXIR	NO
32	16	Settable	0x0000_0080	TIM1	NVIC->ISER[0].16	TIM1_IDE->INTEN	TIM1_IDE->TIE TIM1_IDE->EXFIE TIM1_IDE->EXRIE	TIM1_STS->TIF TIM1_STS->EXIF TIM1_STS->EXIR	NO
33	17	Settable	0x0000_0084	TIM2	NVIC->ISER[0].17	TIM2_IDE->INTEN	TIM2_IDE->TIE TIM2_IDE->EXFIE TIM2_IDE->EXRIE	TIM2_STS->TIF TIM2_STS->EXIF TIM2_STS->EXIR	NO
34	18	Settable	0x0000_0088	TIM3	NVIC->ISER[0].18	TIM3_IDE->INTEN	TIM3_IDE->TIE TIM3_IDE->EXFIE TIM3_IDE->EXRIE	TIM3_STS->TIF TIM3_STS->EXIF TIM3_STS->EXIR	NO
35	19	Settable	0x0000_008C	TIM4	NVIC->ISER[0].19	TIM4_IDE->INTEN	TIM4_IDE->TIE TIM4_IDE->EXFIE TIM4_IDE->EXRIE	TIM4_STS->TIF TIM4_STS->EXIF TIM4_STS->EXIR	NO

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
				TIM5	\	TIM5_IDE->INTEN	TIM5_IDE->TIE TIM5_IDE->EXFIE TIM5_IDE->EXRIE	TIM5_STS->TIF TIM5_STS->EXIF TIM5_STS->EXIR	NO
36	20	Settable	0x0000_0090	TIM6	NVIC->ISER[0].20	TIM6_IDE->INTEN	TIM6_IDE->TIE TIM6_IDE->EXFIE TIM6_IDE->EXRIE	TIM6_STS->TIF TIM6_STS->EXIF TIM6_STS->EXIR	NO
				TIM7	\	TIM7_IDE->INTEN	TIM7_IDE->TIE TIM7_IDE->EXFIE TIM7_IDE->EXRIE	TIM7_STS->TIF TIM7_STS->EXIF TIM7_STS->EXIR	NO
37	21	Settable	0x0000_0094	PWM0	NVIC->ISER[0].21	PWM0_CON->INTEN	\	PWM0_STS>PWMIF	NO
38	22	Settable	0x0000_0098	LEDPWM	NVIC->ISER[0].22	LEDPWM_CON->INTEN	\	LEDPWM_STS>PWMIF	NO
39	23	Settable	0x0000_009C	TWI0	NVIC->ISER[0].23	TWI0_IDE->INTEN	\	TWI0_STS->TWIF	NO
40	24	Settable	0x0000_00A0	TWI1	NVIC->ISER[0].24	TWI1_IDE->INTEN	\	TWI1_STS->TWIF	NO
41	25	Reserved	0x0000_00A4	\	\	\	\	\	
42	26	Reserved	0x0000_00A8	\	\	\	\	\	
43	27	Reserved	0x0000_00AC	\	\	\	\	\	
44	28	Reserved	0x0000_00B0	\	\	\	\	\	
45	29	Settable	0x0000_00B4	ADC	NVIC->ISER[0].29	ADC_CON->INTEN	\	ADC_STS->ADCIF	NO
46	30	Settable	0x0000_00B8	CMP	NVIC->ISER[0].30	\	CMPCFG->CMPIM[1:0]	CMP_STS->CMPIF	YES
47	31	Settable	0x0000_00BC	TK	NVIC->ISER[0].31	TKCON->INTEN	\	TKIF	YES

8 Power Saving Mode

Upon initial power-up, the system runs in Normal Mode. Additionally, three power-saving modes are available:

- Low-Speed Mode: The system clock source can be LIRC, and the CPU can operate at 32KHz.
- IDLE Mode: The system can be awakened by any interrupt.
- STOP Mode: The system can be awakened by INT0~15, Base Timer, TK, and CMP.

9 GPIO

9.1 Clock Source

M0+ core can achieve single-cycle access to GPIO through the IOPORT bus, resulting in highly efficient data transfer. The IOPORT bus clock is derived from HCLK.

9.2 Feature

The GPIO port features of the SC32F10T/10G series are as follows:

- A maximum of 46 bidirectional independently controlled GPIOs
- CPU can access GPIO ports through the IOPORT bus in a single cycle
- Independent setting of pull-up resistors
- All ports have four levels of source driving capability
- All I/Os have high sink current driving capability (50mA)
- 16 I/Os in one group
- Whether input mode or output mode, reading from the port data register retrieves the actual status value of the port

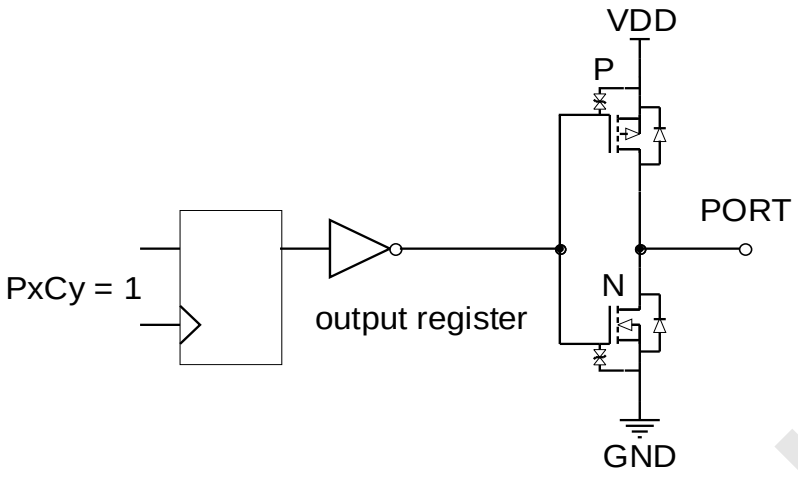
Note: Unused and non-exported ports should be set to strong push-pull output mode

9.3 GPIO Structure Diagram

Strong Push-pull Output Mode

In the strong push-pull output mode, it can provide continuous high-current drive: an output greater than 10mA is high, and an output greater than 50mA is low.

The schematic diagram of the port structure of the strong push-pull output mode is as follows:

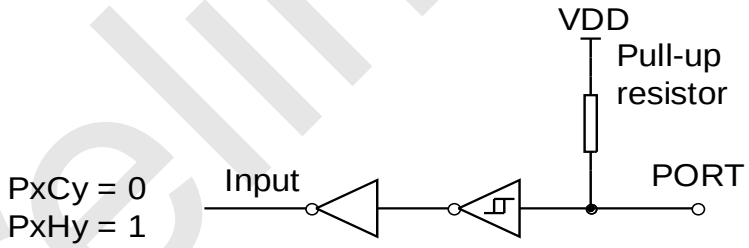


Strong push-pull output mode

Pull-up Input Mode

In the pull-up input mode, a pull-up resistor is constantly connected to the input port. Only when the input port is pulled low, the low-level signal is detected.

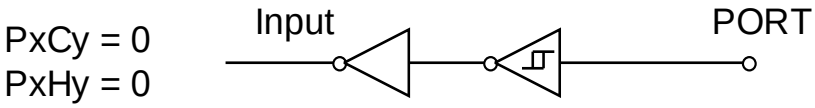
The schematic diagram of the port structure with pull-up input mode is as follows:



Input mode with pull-up resistor

High Impedance Input Mode (Input only)

The schematic diagram of the port structure of the high impedance input mode is as follows:



High impedance input mode

10 Analog-to-Digital Converter ADC

10.1 Clock source

- The SC32F10T/10G series ADC has only one clock source, which is derived from PCLK
- Fixed conversion time of 950ns

10.2 Feature

- Precision：14 bits
- Maximum Channels: Supports up to 13 channels, including 12 external ADC sampling channels and other functions multiplexed with I/O ports. Additionally, one internal ADC channel can directly measure the VDD voltage
- Built-in Reference Voltages: 2.4V,2.048V, and 1.024V
- Reference Voltage Selection: VDD,2.4V,2.048V and 1.024V
- Direct Measurement of VDD: The internal ADC can directly measure the VDD voltage
- ADC Input Channel Selection: Can be configured through the ADCIS[4:0] bits.
- Software-Triggered Conversion: The conversion process can be initiated by software
- Interrupt Support: Configurable ADC conversion completion interrupt
- Conversion Time: Sampling to completion time as low as 2μs
- DMA Transfer Support: ADC conversion completion can generate a DMA request
- Single-Channel Continuous Conversion Mode Support: Allows continuous conversion in single-channel mode
- Overflow Flag: The ADC conversion result supports an overflow flag, and the OVERRUN flag is in the same register (ADCV), allowing the user to read both at once

10.3 ADC Conversion Steps

The actual operation steps required for the user to perform ADC conversion are as follows:

① Set the ADC input pin; (set the bit corresponding to AINx as ADC input, usually the ADC pin will be fixed in advance);

② Set ADC reference voltage Vref, set the frequency used for ADC conversion;

③ Set ADCEN to enable the ADC module power supply;

④ Select ADC input channel; (set ADCIS bit, select ADC input channel);

⑤ Start ADCS and start conversion;

⑥ Wait for EOC/ADCIF=1. If the ADC interrupt is enabled, the ADC interrupt will be generated. The user needs to clear the EOC/ADCIF flag by software;

⑦ Get 14-bit data from ADCV, then one conversion is completed;

⑧ If the input channel is not changed, continuous conversion mode can be set by setting CONT to 1 through software. The conversion will continue until this bit is cleared to 0;

⑨ When the ADC conversion result overflows, the OVERRUN flag will set to 1;

⑩ Conversion data can be transferred using DMA;

11 Analog Comparator CMP

The SC32F10T/10G series features a built-in analog comparator (CMP), and CMP interrupt can wake up the STOP Mode. It can be used for applications such as alarm circuits, power supply voltage monitoring circuits, zero-crossing detection circuits, etc.

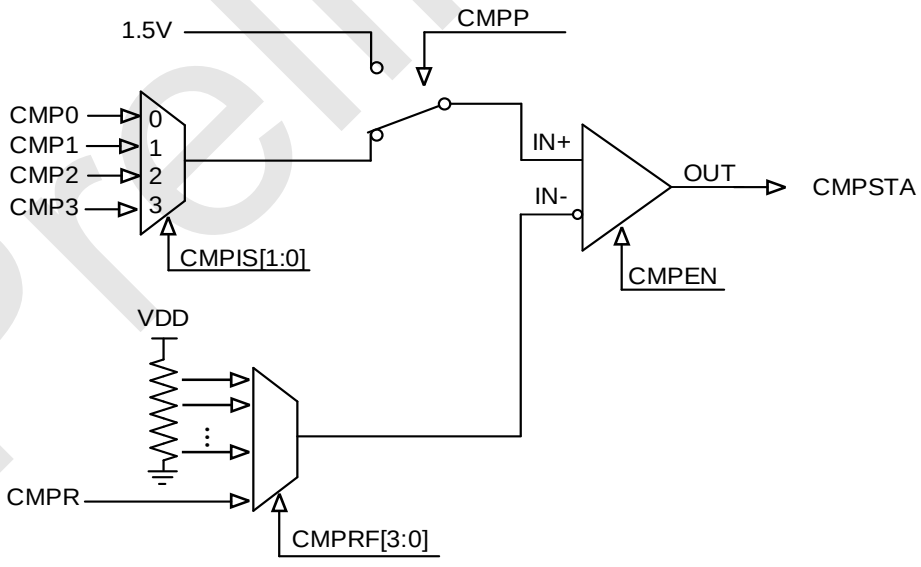
The comparator has four analog signal positive input terminals: CMP0~3, which can be selected through CMPIS [1:0]. The negative input terminal voltage can be switched through CMPRF[3:0] to an external voltage on the CMPR pin or one of the 16 reference voltages internally.

The interrupt mode of the comparator can be conveniently set using CMPIM[1:0]. When the interrupt condition set by CMPIM[1:0] occurs, the comparator interrupt flag CMPIF will set to 1. This interrupt flag needs to be cleared by software.

11.1 Feature

- Four analog signal positive input terminals: CMP0~CMP3
- Negative input voltage can be selected from CMPR handover or one of the 16 comparison voltages derived from the internal VDD division
- CMP interrupt can wake up the STOP Mode

11.2 Analog Comparator Structure Diagram



Analog Comparator Structure Diagram

12 UART0~3

12.1 Clock Source

The SC32F10T/10G series UART has only one clock source, which is derived from PCLK

12.2 Feature

- Four UARTs，UART0~3
  - UART2 can be mapped to another set of ports
- Each UART has three communication modes to choose from:
  - Mode 0: 8-bit half-duplex synchronous communication mode, serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits or receives 8 bits, with the low bit transmitted or received first
  - Mode 1: 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. The communication baud rate is variable
  - Mode 3: 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, 1 programmable 9th bit and 1 stop bit. The communication baud rate is variable
- Interrupts will be generated and corresponding flags TXIF and RXIF will be set when transmission and reception are complete. Interrupt flags need to be cleared by software
- UART0 and UART1 can generate DMA requests
- UART2 and UART3 cannot generate DMA requests
- Independent baud rate generator
- Supports waking up from STOP Mode:
  - The falling edge of the START bit can wake up STOP Mode
  - Provides corresponding wake-up interrupt enable bit WKIE and wake-up interrupt flag WKIF

13 SPI0~1

13.1 Clock Source

The SC32F10T/10G series SPI has only one clock source, which is derived from PCLK

13.2 SPI0 Feature

- Supports 11-stage SPI clock pre-scaling, allowing users to set to lower frequencies
- Signal ports can be mapped to two additional sets of ports
- Features a 16-bit 8-level FIFO with independent transmission and reception
  - SPI0's FIFO function allows continuous writing of 8 or fewer 8-bit or 16-bit transmit data to the SPI send buffer (SPI0_DATA). During SPI transmission, the data written into the FIFO first is also sent first. When the data written by the user to the FIFO is sent, the FIFO empty flag TXEIF will be set; if the FIFO is full, the write conflict flag WCOL will be set, and the user cannot write data to the FIFO until the data in the FIFO is sent out

and the FIFO is not full. The interrupt flag SPIF will be set only when all the data in the FIFO has been sent

- Continuously read 8 or fewer 8-bit or 16-bit receive data from the SPI receive buffer (SPI0_DATA), with the first received data being the first to be read
- FIFO data transfer half-interrupt and corresponding flags for timely reading/writing of data:
  - Provides an interrupt and corresponding flag TXHIF when there is less than half of the valid data in the transmit FIFO
  - Provides an interrupt and corresponding flag RXHIF when there is more than half of the data in the receive FIFO
- Support recieve buffer overflow interrupt and corresponding flag to promptly notify exceptions

- Support DMA
  - Enable TXDMAEN, and the DMA request can be triggered after the transmit buffer empty flag TXEIF is set. After DMA writes to the transmit buffer, the TXEIF flag is automatically cleared
  - Enable RXDMAEN, and the DMA request can be triggered after the receive buffer not empty status flag RXNEIF is set. After DMA reads from the receive buffer, the RXEIF flag is automatically cleared

13.3 SPI1 Feature

- Supports 11-stage SPI clock pre-scaling, allowing users to set to lower frequencies
- Signal ports can be mapped to one additional sets of ports
- No FIFO
- Supports DMA: A request is uniformly set at the end of a frame

13.4 SPI0 and SPI1 Comparison

Comparison BIT	SPI0	SPI1
WCOL	When the send FIFO is full, attempting to write to the FIFO will fail, and WCOL will be set, indicating a buffer write conflict	When one frame is sending, attempting to write to the FIFO will fail, and WCOL will be set, indicating a buffer write conflict
SPIF	This position being set indicates the completion of receiving/sending one frame of data	This position being set indicates the completion of receiving/sending one frame of data
RXHIE	Interrupt enable bit for the valid data in the recieve FIFO is more than half	None
TXHIE	Interrupt enable bit for the valid data in the transmit FIFO is less than half	None
RXIE	Interrupt enable bit for the receive FIFO full	None
TBIE	Interrupt enable bit for the transmit FIFO empty	Interrupt enable bit for the transmit FIFO empty
RXNEIE	Interrupt enable bit for the receive FIFO not empty	None
RXHIF	Set when the valid data in the receive FIFO is more than half	None
TXHIF	Set when the valid data in the receive FIFO is less than half	None
RXFIF	Set when the receive FIFO is full	None

Comparison / BIT	SPI0	SPI1
TXEIF	Set when the receive FIFO is empty	Set when the receive FIFO is empty
RXNEIF	Recieve FIFO not empty flag	None
DMA	Triggering DMA requests through the TXEIF flag and the RXNEIF flag	A request is uniformly set at the end of a frame

14 TWI0~1

14.1 Clock Source

The SC32F10T/10G series TWI has only one clock source, which is derived from PCLK

14.2 Feature

- Support 2 sets of TWI interfaces: TWI0 and TWI1
- Support TWI signal mapping
  - TWI0 can be mapped to three other groups of IO
  - TWI1 can be mapped to two other groups of IO
- Support master/slave mode
- Bidirectional data transmission between master and slave
- Communication speed can reach up to 1 Mbps
- Optional clock extension
- Support DMA
  - TWI0 can generate DMA requests
  - TWI1 cannot generate DMA requests

14.3 TWI Signal Description

On the TWI bus, data is synchronously transmitted between the master and slave devices using the clock line (SCL) and the data line (SDA). Each data byte has a length of 8 bits, and one data bit is transferred with each SCL clock pulse. The data is transmitted starting from the most significant bit (MSB), and after each byte, an acknowledgment bit follows. Each bit is sampled when SCL is high. Therefore, the SDA line may change when SCL is low, but it must remain stable when SCL is high. When SCL is high, any transition on the SDA line is considered a command (START or STOP)

TWI Clock Signal Line(SCL):

The clock signal is generated by the master and is connected to all the slaves. It transmits one byte of data every 9 clock cycles. The first 8 cycles are used for data transmission, and the last one is used as the acknowledgment clock for receiver. It should be pulled up by the pull-up resistor on the SDA line when idle.

TWI Data Signal Line(SDA)

SDA is a bidirectional signal line and should be pulled up by the pull-up resistor on the SDA line when idle.

15 Hardware Watchdog WDT

The SC32F10T/10G series features a built-in hardware watchdog (WDT) with an internal 32kHz oscillator as its clock source. Users can choose to enable the watchdog reset function by setting the ENWDT control bit in the Code Option through a programmer.

15.1 Clock Source

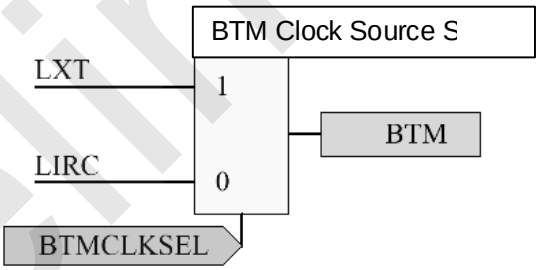
The SC32F10T/10G series WDT is fixed to LIRC. Once the WDT is enabled, LIRC will automatically start, and it will remain oscillating throughout the operation of the WDT and users cannot turn off LIRC while the WDT is active.

16 Base Timer（BTM）

The SC32F10T/10G series features a Base Timer (BTM) that can generate interrupts at intervals ranging from 15.625ms to 32s. The BTM can use either 32kHz LIRC or external 32.768kHz crystal oscillator (LXT) as its clock source. The interrupts generated by the BTM can wake up the CPU from STOP mode.

16.1 Clock Sourse

SC32F10T/10G series BTM can choose LXT or LIRC as its clock sourse



16.2 Feature

- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

17 Built-in CRC Module

The SC32F10T/10G series has a built-in CRC (Cyclic Redundancy Check) module that utilizes a polynomial generator to generate CRC codes from an 8-bit/16-bit/32-bit data word.

17.1 Clock Source

The SC32F10T/10G series CRC has only one clock source, which is derived from PCLK.

17.2 Feature

- 1 built-in hardware CRC module
- Configurable initial value, with a default of 0xFFFFFFFF
- Supports 8-bit/16-bit/32-bit data units
- Programmable polynomial, with a default of 0x4C11DB7
- Only supports software-driven data computation mode
- Supports DMA: CRC_DR can serve as the DMA destination address or be accessed directly via registers
- Calculating CRC for a single byte requires 1 system clock

CRC algorithm	CRC-32/MPEG-2
Polynomial Formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$
Data Width	32bit
Inital Value	0xFFFFFFFF
Result XOR Value	0x00000000
Input Value Reversal	false
Output Value Reversal	false
LSB/MSB	MSB

Note: The written and read data in CRCDR cannot be the same.

18 PWM0: 8 Channels of 16-bit Multifunctional PWM

18.1 Clock Source

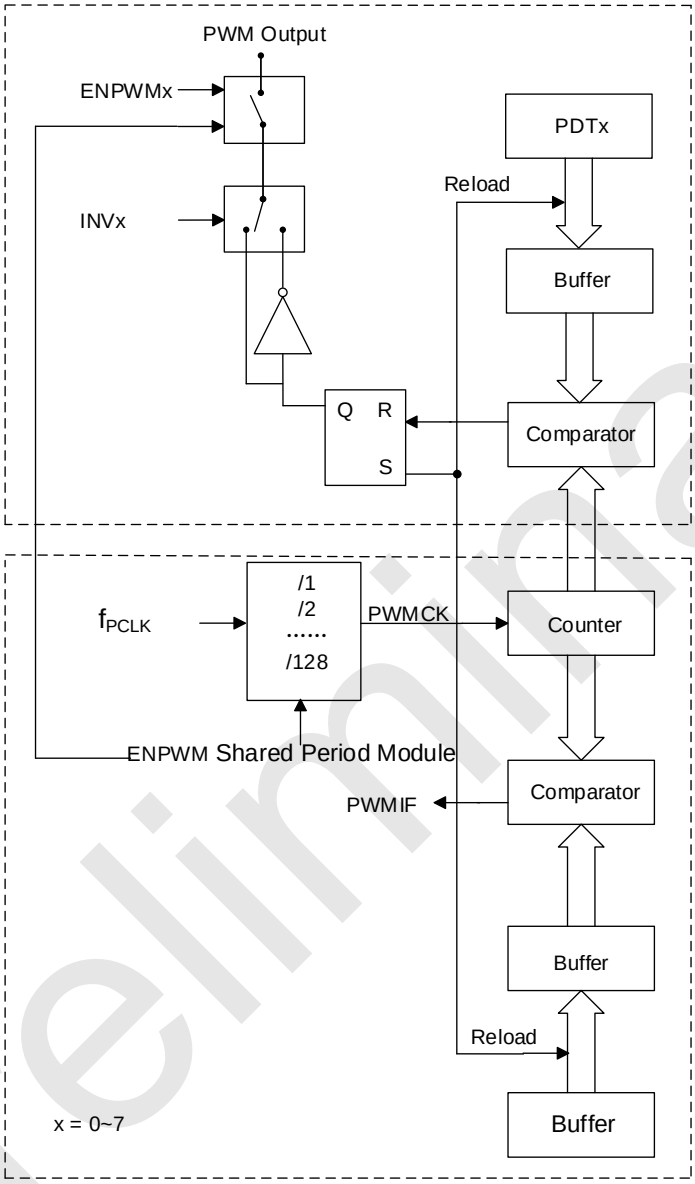
The SC32F10T/10G series PWM0 has only one clock source, which is derived from PCLK

- PWM0 output frequency is at its maximum the frequency of the selected clock source
- PWM0 clock pre-scaler can select from 1 to 128

18.2 Feature

- 8 channels of 16-bit shared-period multifunctional PWM
- The output waveform can be inverted
- Waveform types: can be set as center-aligned or edge-aligned
- PWM modes: can be set as independent mode or complementary mode:
  - In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
  - In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously
- Provides one PWM overflow interrupt
- Supports fault detection
- Has independent interrupt request flags

18.3 PWM0 Structure Diagram



PWM0 Structure Diagram

18.4 PWM0 General Configuration

18.4.1 Output Mode

- In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
- In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously

18.4.2 Alignment Type

- Edge-aligned
- Center-aligned

18.4.3 Duty Cycle Change Characteristics

When generating the PWM0n output waveform, if it is necessary to change the duty cycle, it can be achieved by modifying the high-level setting register (PDT0x). However, it is important to note that changing the value of PDT0x will not immediately alter the duty cycle. Instead, the change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.

18.4.4 Period Change Characteristics

When generating PWM output waveforms, if it is necessary to change the period, it can be achieved by modifying the period setting register PWMPD. Similar to the duty cycle, changing the value of PWMPD will not immediately alter the period. The change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.

19 LEDPWM: 8 Channels of 32-bit LEDPWM

19.1 Clock Source

The SC32F10T/10G series LEDPWM has only one clock source, which is derived from PCLK2.

19.2 Feature

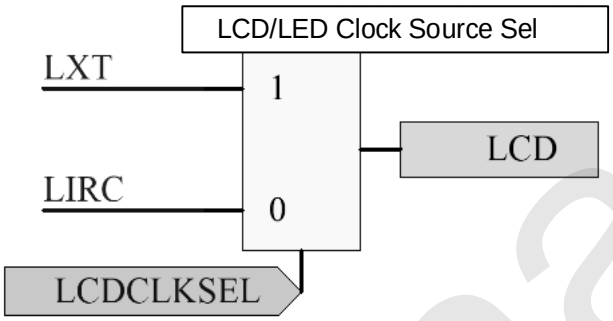
- Shared period and independently adjustable duty cycle
- Support center-aligned mode for driving LEDs conveniently
- Duty cycle register shares with 28 SEG registers, serving as an alternative to LED circuits, generating LED driving waveforms
- The highest pre-scaling option is /256, with each step being 2^n
- Support independent interrupt request flags
- Achieve grayscale adjustment through center-aligned LEDPWM：
  - In grayscale adjustment, one COM corresponds to a maximum of 28 duty values, offering options like 8 X 24, 6 X 26, 5 X 27, 4 X 28
  - During LEDPWM interrupts, switch COM and write corresponding duty value into DUTY register of LEDPWM can achieve the adjustment of each SEG’s grayscale.

20 LCD/LED Driver

LCD/LED option, sharing registers and I/O ports

20.1 Clock Source

SC32F10T/10G series LCD/LED can choose LXT or LIRC as its clock sourse



20.2 Built-in 8 COM x 24 SEG LED Driver

- 1/1~1/8 duty voltage driving mode
- LED segment source driving capability with four-level control

20.3 Built-in 8 COM x 24 SEG LCD Driver

- Type A / Type B waveform selectable
- 8 X 24、6 X 26、5 X 27、4 X 28
- Optional voltage division resistor for LCD voltage output port
- LCD display driver bias voltage
  - 1/4 bias voltage
  - 1/3 bias voltage
- Three selectable frame rates:
  - Type A mode 32/64/128Hz
  - Type B mode 64/128/256Hz

21 32-Channel High-Sensitivity Touch Key Circuit(TK)

- High-sensitivity mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Channels can be scanned in parallel
- Support self-capacitance mode and mutual-capacitance mode
- Support low-power mode
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

Note: Exclusive to the SC32F10T series

22 16-bit Timers (Timer0~Timer7)

22.1 Clock Source

- In timer mode/PWM output mode, the TIM clock source is derived from PCLK
- In counter mode, the Tn pin serves as the counting source input

22.2 Feature

- 8 independent 16-bit auto-reload counters: Timer0 to Timer7
- 16-bit incremental, decremental, and increment/decrement auto-reload counters
- Support rising/falling edge capture, enabling PWM duty and period capture
- 16-bit programmable prescaler, allowing division of the counter clock frequency by any number between 1 and 65535
- Overflow and capture events of TIM1/2/6 can generate DMA requests
- TIM2/3/7 pins can be remapped:
  - TIM2
    - 0: T2CAP/T2 pin is PA10
    - 1: T2CAP/T2 pin is PA12
  - TIM3
    - 0: T3CAP/T3 pin is PA0
    - 1: T3CAP/T3 pin is PA13
  - TIM7
    - 0: T7CAP/T7 pin is PC1
    - 1: T7CAP/T7 pin is PB1

22.3 Counting method

- Upward Counting: Counts from the set value upwards to overflow at 0xFFFF
- Downward Counting: Counts from 0xFFFF downwards to the set value

22.4 Timer Signal Port

- Tn, n=1~7
  - Clock input/output
  - Both rising and falling edges can be captured
- TnEX, n=0
  - In reload mode, the external event input (falling edge) on the TnEX pin is used for reload enable/disable control
  - In capture mode, when FSEL = 1, it serves as a falling edge capture signal input. Detection of a falling edge on the TnEX pin generates a capture, sets EXIF, and captures the value of the TnCNT register into the FCAP register
- TnPWM, n=0~7
  - TIM1~7 can provide PWM with independently adjustable duty cycle through the Tn port: TnPWMA
  - TIM0 can provide PWM with independently adjustable duty cycle through the TnEX port: TnPWMB
  - Optional clock source follows TIM
  - Note: TIM's PWM capture function and PWM output function cannot be enabled simultaneously

22.5 Interrupts and Corresponding Flags for TIM:

- Overflow/underflow of the counter share the interrupt flag TIF
- Capture status flags:
  - EXIF: Flag indicating detection of a falling edge on the external event input
  - EXIR: Flag indicating detection of a rising edge on the external event input
- Interrupt and priority configuration control bits are merged into the NVIC module

23 Direct Memory Access (DMA)

23.1 Overview

The DMA controller is designed for high-speed data transfer, allowing the movement of data from one address to another without the need for CPU intervention. Leveraging DMA for data transfer can reduce the workload on the CPU, enabling the saved CPU resources to be utilized for other applications. The DMA controller comprises 4 channels, each directly connected to dedicated hardware DMA requests. Additionally, each channel supports software triggering. The DMA controller features support for 4-level channel priority, facilitating the management of priority between DMA requests to ensure that only one DMA channel operates at any given time. It also supports both single and batch transfers, with the request source being either a software request or an interface request. Data transfer between memories is accomplished using software requests.

Note: For a bidirectional data transfer application, two DMA channels are required to handle sending and receiving operations.

23.2 Clock Source

The clock source of DMA is derived from HCLK, and the external peripheral clock of DMA is enabled through

AHB_CFG.DMAEN.

23.3 Feature

- Support 4 independent configurable channels
- Support 4 priority levels for requests
- Support 8-bit, 16-bit, 32-bit data transfers
- Support automatic increment/decrement or fixed source and destination addresses, with data widths of byte, half-word, and word
- Support single and burst transfer modes

23.4 Function Description

23.4.1 Transmission

No transmit limitation between peripheral and memory for DMA：

Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory	Peripheral-to-Periphral
No limitation	No limitation	No limitation	No limitation

23.4.2 DMA Access Restriction

Users are not allowed to perform write operations on Flash or access the core through DMA. Violating these restrictions may lead to unpredictable exceptions.

23.4.3 Channel Priority

There are 4 priority levels can be configured through PL[1:0] registers:

- 00: Low
- 01: Medium
- 10: High
- 11: Very High

23.4.4 Single Transmission and Burst Transmission

The DMA controller supports single and burst data transfer types, and the request source can be a software request or an interface request while data transfer between memory is done by software requests. Single transfer means that the software or interface is ready to transfer one data (each data requires one request), while burst transfer means that the software or interface will transfer multiple data (multiple data requiring only one request).

The modes of single and burst transfer can be set through TPTYPE register (DMAn_CFG[15]).

In single transfer mode, each transfer of data requires one request. As each data is transferred, the values in the register DMAn_CNT[31:0](n=0~3) decrease by 1, the transfer of data is completed when the count in DMAn_CNT[31:0]

becomes 0. In this mode, BURSIZE (DMAn_CFG[14:12]) is not used to control the size of the transferred data and its value is fixed at 1.

In burst transfer mode, DMA transfer DMAn_CNT[31:0] data with only one request. After transferring BURSIZE (DMAn_CFG[14:12]) data, the value in DMAn_CNT[31:0] is decreased by BURSIZE. The transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0.

23.4.5 Loop Mode

The loop mode can be used to handle circular buffers and continuous data streams (such as ADC scan mode). During the loop mode transfer, the number of data to be transferred will automatically reload to the initial value set in the channel configuration phase and continue to respond to DMA requests. To stop loop transfer, the software needs to stop the generation of DMA requests by the peripheral before disabling the DMA channel (for example, exiting ADC scan mode). The software must explicitly set the DMACNT value before starting/enabling the transfer and after stopping the loop transfer.

The SC32F10T/10G series DMA controller supports normal mode and loop mode:

- When CIRC=0 (DMA channel is in non-loop mode), it will no longer accept any DMA requests after reaching the set number of data to be transferred
- When CIRC=1 (DMA channel is in loop mode), after the transfer is complete, the DMACNT of the channel will automatically reload the previously set value and wait for the next loop

Users can flexibly choose according to their actual needs.

24 SysTick

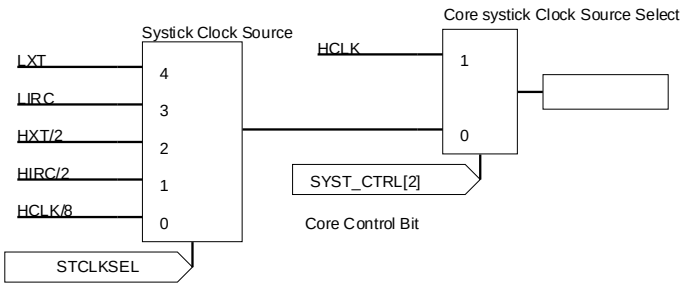
SysTick is a simple, 24-bit, writable-clear, decrementing automatic reload counter with a flexible control mechanism. This counter can be used as a tick timer for a Real-Time Operating System (RTOS) or as a simple counter.

24.1 Clock Source

SysTick (Cortex®-M0+ Core System Timer) has internal clock source and external clock source：

- Internal clock source: CPU Clock
- 5 external clock sources

SysTick clock sourse diagram is as follow:



24.2 SysTick Calibration Register Default Value

The calibration value for the SysTick Calibration Register is set as follows:

- If the default clock after power-on is fHCLK/n (MHz), where n is the default power-on divider, and the default clock source is HIRC
- Then, setting the initial SysTick calibration value to 1000 * (fHCLK/n) will generate a 1ms time reference

25 Electrical Characteristics

Unless otherwise specified, the electrical data in this section are based on the working conditions listed in the "Recommended Operating Conditions" subsection.

25.1 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	Operating voltage 1	2.0	5.5	V	f_{HCLK}=32MHz Clock source is HIRC
T_A	Ambient temperature	-40	105	℃	

25.2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	5.5	V
V_{PIN}	Input/output voltage of any pin	-0.3	V_{DD}+0.3	V
T_A	Ambient temperature	-40	105	℃
T_{STG}	Storage temperature	-55	125	℃
I_{VDD}	Current value flowing through VDD	-	200	mA
I_{VSS}	Current value flowing through VSS	-	200	mA

25.3 Flash ROM Parameters

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
N_{END}	Endurance earse/write cycles	100,000	-	-	Cycles	f_{HCLK}=32MHz Clock source is HIRC
T_{DR}	Data retention time	100	-	-	Years	
$T_{S\text{-}Erase}$	Single sector erase time	-	5	-	ms	
T_{Erase}	Page erase time	30	-	40	ms	
T_{Write}	Single byte write time	-	28	-	μs	

25.4 Power Consumption

25.4.1 V_{DD} = 5V,T_A = +25℃,unless otherwise specified

Symbol	Parameter	Boot Area	Min	Typical	Max	Unit	Conditions
I_{op}	Operating current	APROM	-	6.3	-	mA	f_{HCLK}=32MHz Clock source is HIRC
			-	4	-	mA	f_{HCLK} =16MHz Clock source is HIRC
			-	2.7	-	mA	f_{HCLK} =8MHz Clock source is HIRC
			-	2	-	mA	f_{HCLK} =4MHz Clock source is HIRC
			-	1.6	-	mA	f_{HCLK} =2MHz Clock source is HIRC
I_{op_PD}	STOP Mode current	APROM	-	3.0	-	μA	
I_{op_IDLE}	IDLE Mode current	APROM	-	2.7	-	mA	f_{HCLK} =32MHz Clock source is HIRC

25.4.2 V_{DD} = 3.3V,T_A = +25℃,unless otherwise specified

Symbol	Parameter	Boot Area	Min	Typical	Max	Unit	Conditions
I_{op}	Operating current	APROM	-	6.2	-	mA	f_{HCLK}=32MHz Clock source is HIRC
			-	4	-	mA	f_{HCLK} =16MHz Clock source is HIRC
			-	2.7	-	mA	f_{HCLK} =8MHz Clock source is HIRC
			-	2	-	mA	f_{HCLK} =4MHz Clock source is HIRC
			-	1.6	-	mA	f_{HCLK} =2MHz Clock source is HIRC
I_{op_PD}	STOP Mode current	APROM	-	3.0	-	μA	
I_{op_IDLE}	IDLE Mode current	APROM	-	2.6	-	mA	f_{HCLK} =32MHz Clock source is HIRC

25.5 GPIO Parameter

25.5.1 V_{DD} = 5V,T_A = +25℃,unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH}	Input high voltage	0.7V_{DD}	-	V_{DD}+0.3	V	
V_{IL}	Input low voltage	-0.3	-	0.3V_{DD}	V	
V_{IH_ST}	Schmitt trigger input high voltage	0.8V_{DD}	-	V_{DD}	V	Schmitt trigger input: NRST T_CLK / T_DIO UART0 enter RX0 SPI / TWI signal input INT0~INT15 PWM fault detection port FLT Timer clock input Tn Timer capture port TnEX
V_{IL_ST}	Schmitt trigger input low voltage	-0.2	-	0.2V_{DD}	V	
I_{OL}	Output low current @V_{Pin}=0.4V	-	27	-	mA	V_{Pin}=0.4V
	Output low current @V_{Pin}=0.8V	-	50	-	mA	V_{Pin}=0.8V
I_{OH}	Output high current @ V_{Pin}=4.3V	-	10	-	mA	Pxyz=0,I_{OH} level 0
		-	8	-	mA	Pxyz=1,I_{OH} level 1
		-	5	-	mA	Pxyz=2,I_{OH} level 2
		-	3	-	mA	Pxyz=3,I_{OH} level 3
	Output high current @ V_{Pin}=4.7V	-	4	-	mA	Pxyz=0,I_{OH} level 0
		-	3	-	mA	Pxyz=1,I_{OH} level 1
		-	2	-	mA	Pxyz=2,I_{OH} level 2
		-	1	-	mA	Pxyz=3,I_{OH} level 3
R_{PH}	Pull-up resistance	-	30	-	kΩ	

25.5.2 V_{DD} = 3.3V,T_A = +25℃, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH}	Input high voltage	0.7V_{DD}	-	V_{DD}+0.3	V	
V_{IL}	Input low voltage	-0.3	-	0.3V_{DD}	V	
V_{IH_ST}	Input high voltage	0.8V_{DD}	-	V_{DD}	V	Schmitt trigger input: NRST T_CLK / T_DIO UART0 enter RX0 SPI / TWI signal input INT0~INT15
V_{IL_ST}	Input low voltage	-0.2	-	0.2V_{DD}	V	

						PWM fault detection port FLT Timer clock input Tn Timer capture port TnEX
I_{OH}	Output low current @ V_{Pin}=0.4V	-	22	-	mA	V_{Pin}=0.4V
I_{OL}	Output low current @ V_{Pin}=0.8V	-	35	-	mA	V_{Pin}=0.8V
I_{OH}	Output high current @ V_{Pin}=3.0V	-	3	-	mA	Pxyz=0,I_{OH} level 0
		-	2.3	-	mA	Pxyz=1,I_{OH} level 1
		-	1.7	-	mA	Pxyz=2,I_{OH} level 2
		-	1	-	mA	Pxyz=3,I_{OH} level 3
R_{PH}	Pull-up resistance	-	50	-	kΩ	

25.6 AC Electrical Characteristics

(V_{DD} = 2.0V ~ 5.5V,T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
T_{LXT}	External 32kHz oscillator start-up time	-	0.8	-	s	External 32kHz crystal oscillator
T_{POR}	Power On Reset time	-	15	-	ms	
T_{PDW}	STOP Mode wake-up time	-	65	130	μs	
T_{Reset}	Reset pulse width	18	-	-	μs	low-level active
T_{LVR}	LVR debounce time	-	30	-	μs	
f_{HIRC}	HIRC oscillator stability	31.68	32	32.32	MHz	V_{DD}=2.0~5.5V T_A=-40~105 ℃
f_{LIRC}	LIRC oscillator stability	30.72	32	33.28	KHz	V_{DD}=2.0~5.5V T_A=-40~105 ℃

25.7 ADC Characteristics

(T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{ADC}	Supply Voltage	2.7	5.0	5.5	V	Vref = 2.048V
		2.0	5.0	5.5	V	Vref = 1.024V or Vref = V_{DD}
		2.7	5.0	5.5	V	Vref = 2.4V
V_{REF1}	Internal reference 2.048V	2.028	2.048	2.068	V	V_{DD} = 2.7~5.5V
V_{REF2}	Internal reference 1.024V	1.004	1.024	1.044	V	V_{DD} = 2.0~5.5V
V_{REF3}	Internal reference 2.4V	2.38	2.40	2.42	V	V_{DD} = 2.7~5.5V
N_R	Precision	-	14	-	bit	GND≤V_{AIN}≤V_{DD}
V_{AIN}	ADC Input voltage	GND	-	V_{DD}	V	
R_{AIN}	ADC Input resistance	1	-	-	MΩ	V_{IN}=5V
I_{ADC}	ADC conversoin current	-	-	2	mA	ADC Module on V_{DD}=5V
		-	-	1.8	mA	ADC Module on V_{DD}=3.3V
DNL	Differential nonlinear error	-	-	±5	LSB	V_{DD}=5V V_{REF}=5V
INL	Integral nonlinear error	-	-	±5	LSB	
E_Z	Offset error	-	-	±15	LSB	
E_F	Full scale error	-	-	±20	LSB	
E_{AD}	Total absolute error	-	-	±20	LSB	
T_{ADC}	ADC conversion time	-	1.1	1.4	μs	LOWSP[2:0] = 100 f_{HCLK} =32MHz， Clock source is HIRC
		-	1.2	1.5	μs	LOWSP[2:0] = 101 f_{HCLK} =32MHz，

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
						Clock source is HIRC
		-	1.5	1.9	μs	LOWSP[2:0] = 110 f_{HCLK} =32MHz， Clock source is HIRC
		-	2.0	2.6	μs	LOWSP[2:0] = 111 f_{HCLK} =32MHz， Clock source is HIRC

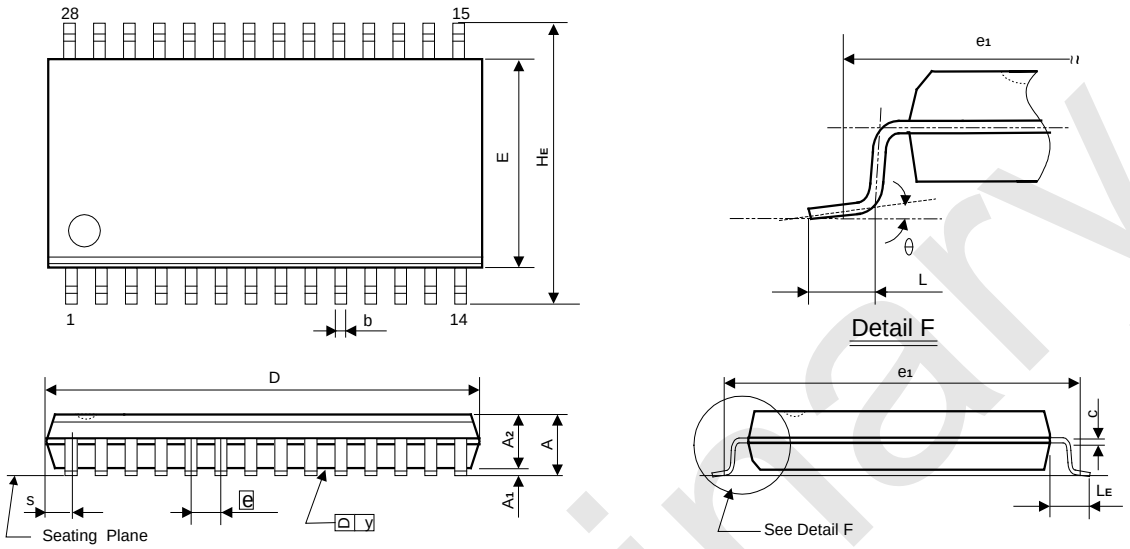
25.8 CMP Electrical Characteristics

(V_{DD} =5V,T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{CM}	Input voltage range	0	-	V_{DD}	V	
V_{OS}	Offset voltage	-	10	30	mV	
V_{HYS}	comparator voltage hysteresis	-	40	-	mV	
I_{CMP}	Comparator switching current	-	-	100	μA	V_{DD}=5V
T_{CMP}	Response time	-	-	2	μs	

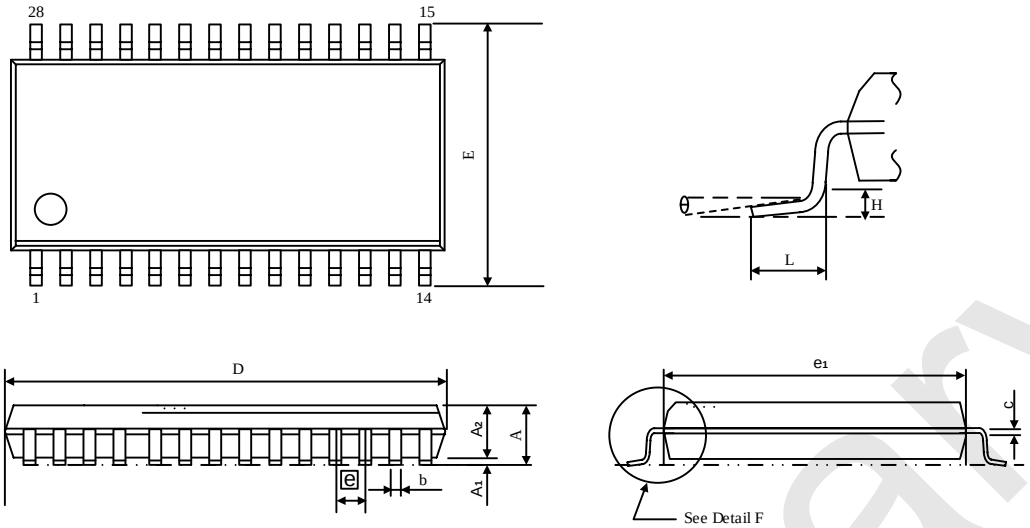
26 Package information

SOP28L(300mil) Dimension Unit: mm



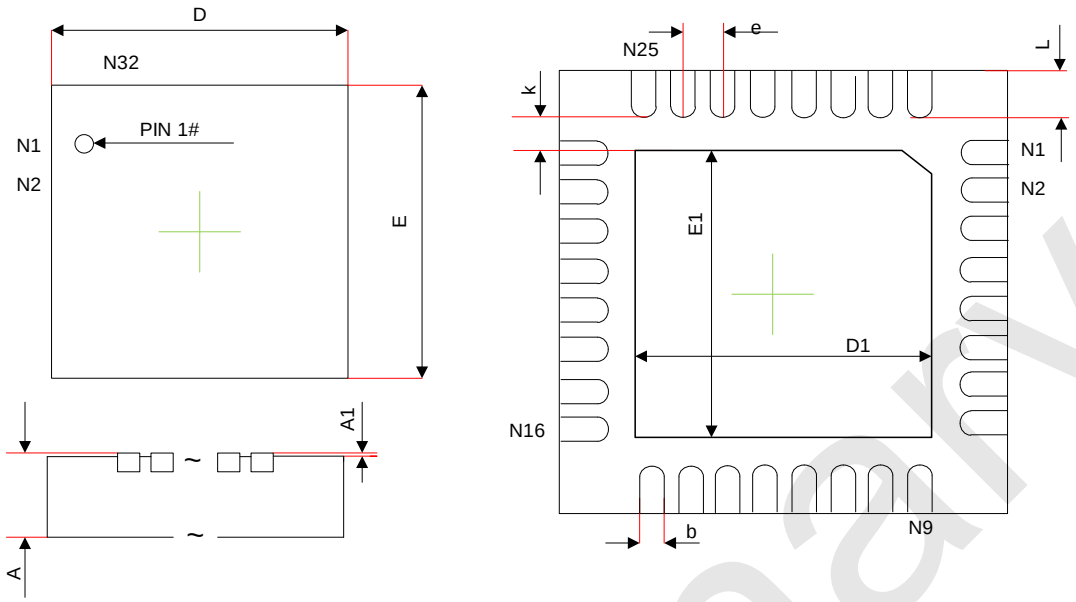
Symbol	mm(milimetre)		
	Min	Normal	Max
A	2.40	2.56	2.65
A**1**	0.100	0.200	0.300
A**2**	2.240	2.340	2.440
b	0.39	---	0.48
C	0.254(BSC)		
D	17.80	18.00	18.20
E	7.30	7.50	7.70
HE	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	0.85	1.0
LE	1.3	1.4	1.5
θ	0°	-	8°

TSSOP28L Dimension Unit: mm



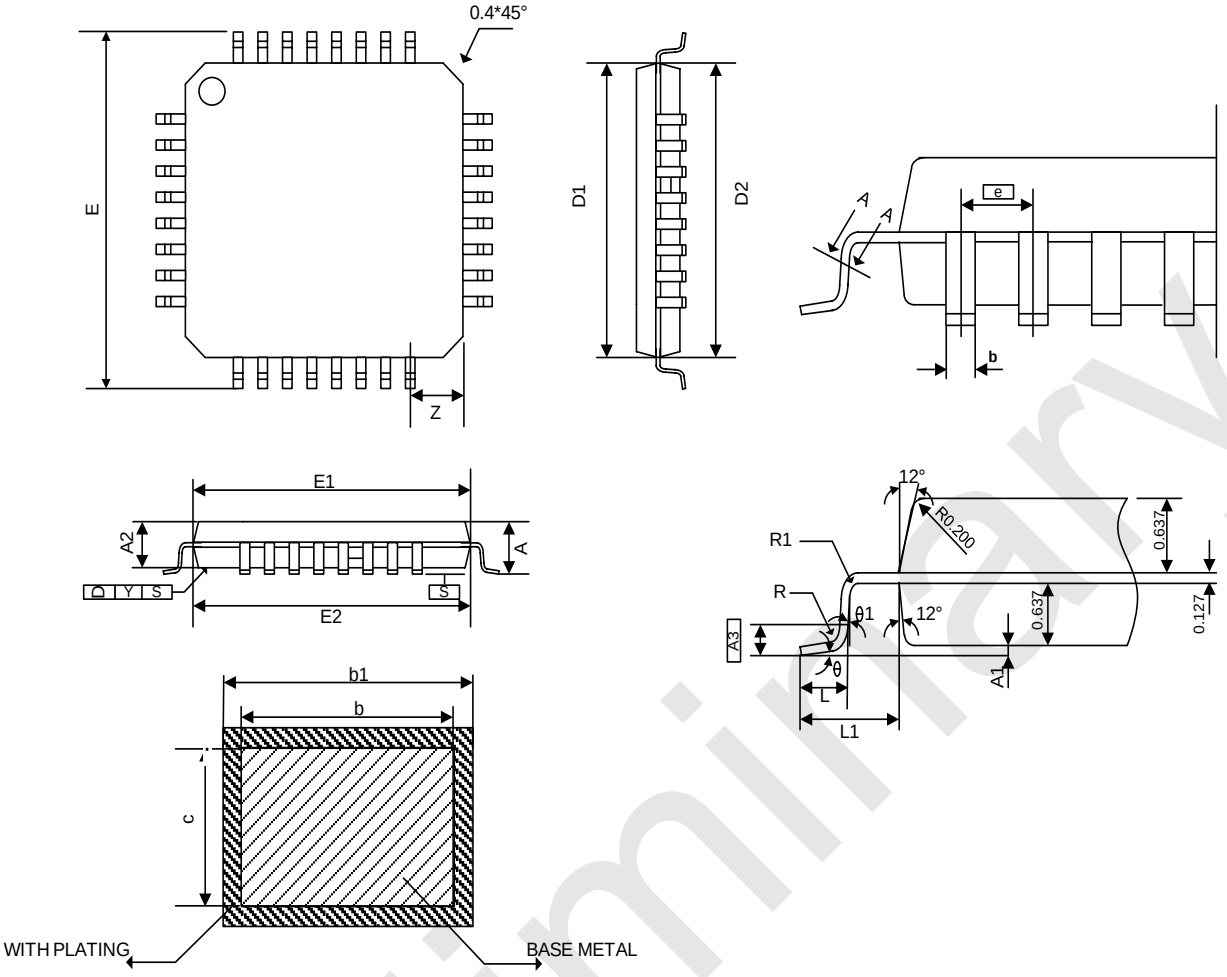
Symbol	mm(milimetre)		
	Min	Normal	Max
A	-	-	1.200
A**1**	0.050	-	0.150
A**2**	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	9.600	-	9.800
E	6.250	-	6.550
e1	4.300	-	4.500
e	0.65(BSC)		
L	-	-	1.0
θ	0°	-	8°
H	0.05	-	0.25

QFN32 (5X5) Dimension Unit: mm



Symbol	mm(milimetre)		
	Min	Normal	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.5 BSC		
k	0.4 REF		
D1	3.30	3.45	3.60
E1	3.30	3.45	3.60
L	0.30	0.40	0.50

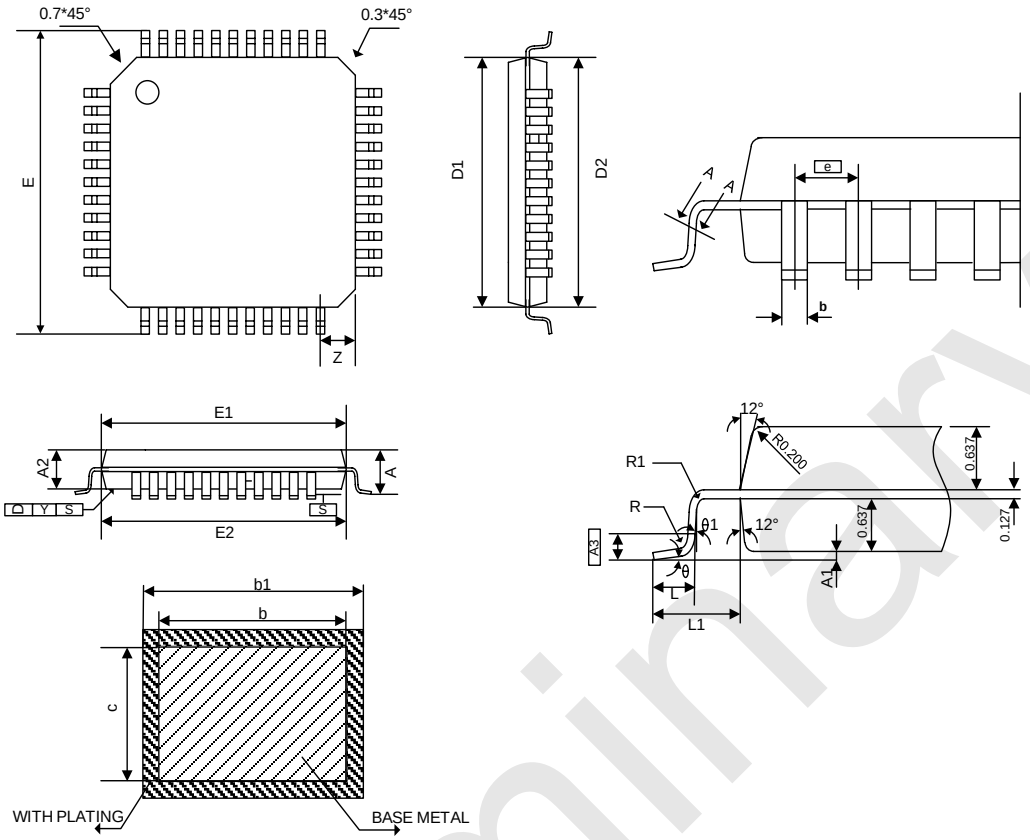
LQFP32 (7X7) Dimension Unit: mm



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.30	1.4	1.5
A3	--	0.254	--
b	0.30	0.35	0.41
b1	0.31	0.37	0.43
c	0.12	0.13	0.14
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	--	0.8	--
L	0.43	--	0.75

Symbol	mm(milimetre)		
	Min	Normal	Max
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.70	--

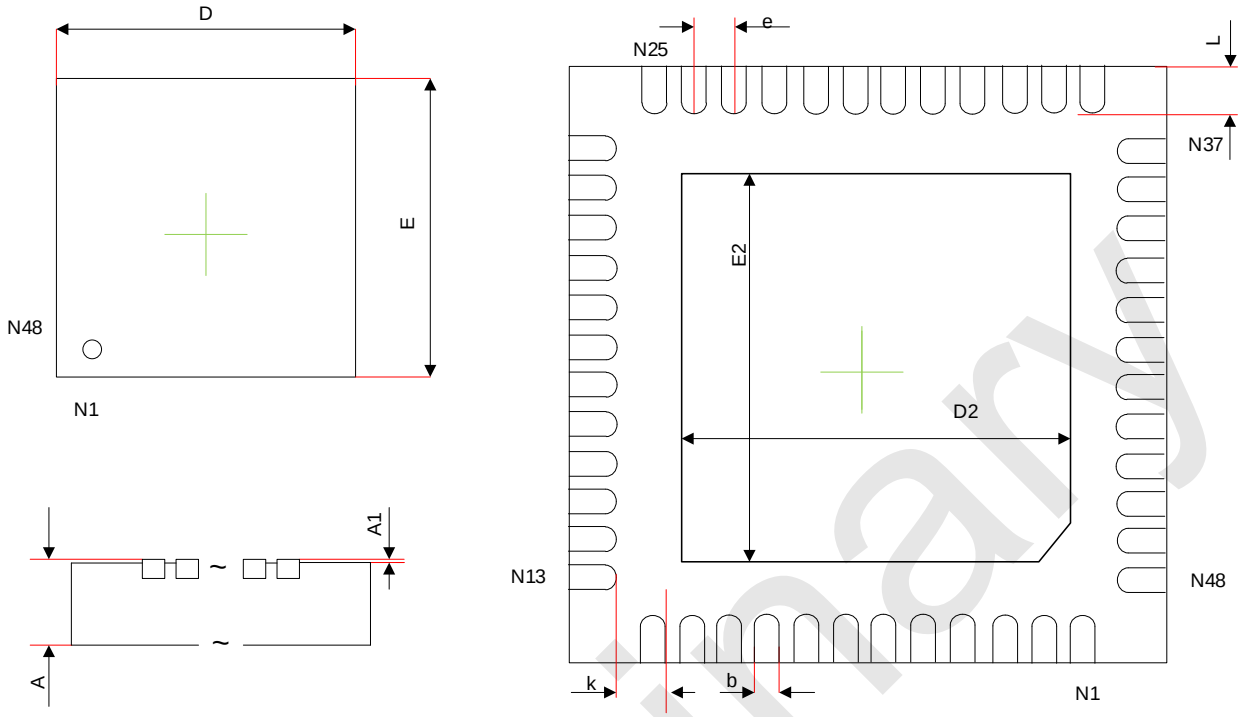
LQFP44 (10X10) Dimension Unit: mm



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.015	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.25	0.30	0.36
b1	0.26	0.32	0.38
c	0.12	0.13	0.14
D1	9.85	9.95	10.05
D2	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.85	9.95	10.05
E2	9.90	10.00	10.10
e	--	0.8	--
L	0.42	--	0.75
L1	0.95	1.0	1.15
R	0.08	--	0.25

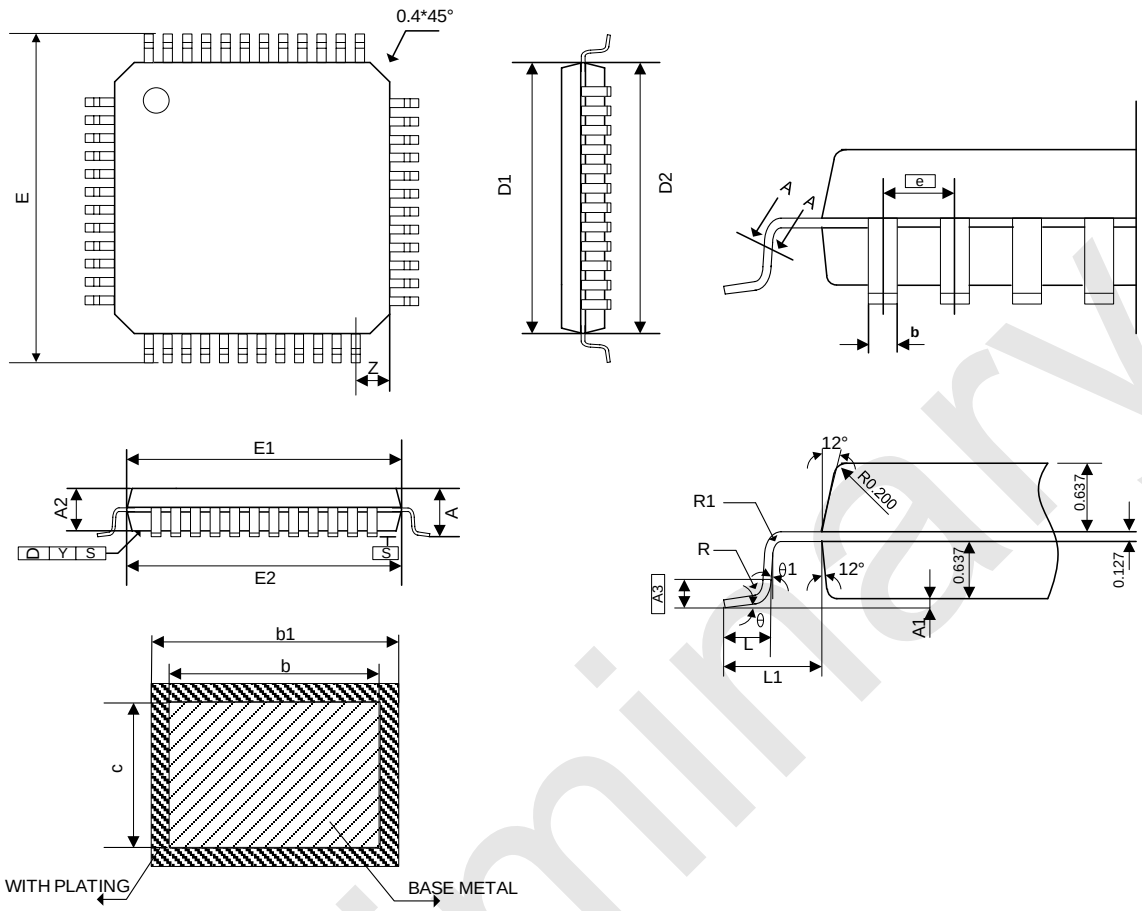
Symbol	mm(milimetre)		
	Min	Normal	Max
R1	0.08	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	1.0	--

QFN48 (5X5) Dimension Unit: mm



Symbol	mm(milimetre)		
	Min	Normal	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.12	--	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35 BSC.		
k	0.20	0.30	--
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40

LQFP48 (7X7) Dimension Unit: mm



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.15	0.20	0.25
b1	0.16	0.22	0.28
c	0.12	--	0.17
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.8	9.00	9.20
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	--	0.5	--
L	0.43	--	0.75

Symbol	mm(milimetre)		
	Min	Normal	Max
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.75	--

27 Revision History

Version	Notes	Date
V0.1	Initial Release	2023.11.30

28 Important Notice

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