

1 General description

The SC32F11T/11G Series comprises industrial-grade Flash microcontrollers based on the Arm Cortex-M0+ Core, featuring integrated touch control and operating at frequencies up to 72 MHz (PLL multiplier). The Cortex-M0+ Core uses a 32-bit Reduced Instruction Set Computer (RISC) architecture compliant with the CMSIS Standard. The SC32F11T/11G Series delivers strong data processing performance with an integrated Direct Memory Access (DMA) controller for high-speed transfers, a hardware CRC module, and a 32-bit hardware multiplier within the core to enhance computation speed.

The SC32F11T/11G Series microcontroller features three clock sources: a high-precision high-frequency oscillator (HIRC), a low-frequency 37 kHz oscillator (LIRC), and a PLL clock. It also provides two external crystal oscillator interfaces: a 2 to 16 MHz high-frequency crystal oscillator (HXT) interface and a 32.768 kHz low-frequency crystal oscillator (LXT) interface. Both the internal clock source and external crystal oscillator interface provide the system clock. The built-in system clock monitor switches the clock source to HIRC upon detecting a system clock failure.

The SC32F11T/11G Series features rich peripherals, including 42 high-sensitivity contactless capacitive touch channels. Up to 60 GPIO pins, all supporting external interrupts. 8 16-bit timers; 8 16-bit multifunction PWM channels with fault detection; 6 independent UARTs supporting master/slave mode. 2 advanced two in one interfaces: QSPI0/1 & SPI0/1 & TWI0/1; 2 general two in one interfaces: SPI2/3 & TWI2/3; built-in LCD/LED hardware drivers. 1 analog comparator, 1 rail-to-rail variable gain amplifier OP/PGA, and 20 channels of 14-bit high-precision ADC; Built-in independent Watchdog Timer (WDT) and Low Voltage Reset (LVR) circuits effectively enhance system reliability; Provides three power modes to meet power consumption requirements across various applications.

The SC32F11T/11G Series offers high performance and high reliability, supporting 2.0-5.5 V operating voltage, capable of operating within an ambient temperature range of -40 °C to 105 °C, and also provides excellent ESD performance and EFT anti-interference capability; In terms of process, the SC32F11T/11G Series utilizes industry-leading eFlash process technology, with Flash write endurance exceeding 100,000 cycles and data retention of 10 years at room temperature; In terms of storage resources, the SC32F11T/11G Series provides up to 512 Kbytes ROM space, up to 32 Kbytes SRAM, with SRAM supporting the parity check function, 1.5 Kbytes user storage area(generic EEPROM), and 4 Kbytes system storage area (LDROM); It includes a built-in system storage area to support OTA upgrades and provides multiple programming methods such as ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application Programming), enabling on-board debugging and firmware updates while the chip is online or powered.

The SC32F11T/11G Series offers excellent touch key features with robust anti-interference performance. It supports diverse touch key and main controller solutions, targeting industrial control and consumer applications such as small and large smart appliances, smart home, Internet of Things, wireless communications, and gaming consoles.

2 Features

Operating conditions

- Operating voltage: 2.0 V to 5.5 V
- Operating temperature: -40 to +105 °C

EMS

- ESD
 - HBM:ANSI/ ESDA/JEDEC JS-001-2024 Class 3A
 - CDM:ANSI/ESDA/JEDEC JS-002-2025 Class C3
- EFT
 - EN61000-4-4 Level 4

Package

- 64 PIN:LQFP64(10X10)
- 48 PIN:LQFP48(7X7)/ QFN48(5X5)
- 44 PIN:LQFP44(10X10)
- 32 PIN:LQFP32(7X7)/ QFN32(4X4)

Core

- Cortex®-M0+ Core
- With Wakeup Interrupt Controller (WIC) module
- 64-bits instruction prefetch
- Integrated multiplier

Reset

- Power-On Reset (POR)
- Software Reset (RST)
- Reset via external NRST pin (PD3) active low
- Watchdog (WDT) Reset
- Low Voltage Reset (LVR)
 - Four selectable reset voltage levels: 4.3 V, 3.7 V, 2.9 V, and 1.9 V
 - The default value is determined by the user's programmed Code Option

Bus

- 1 IOPORT
- 1 AHB
- 3 APBs: APB0-APB2

Power saving mode

- IDLE Mode, can be woken up by any Interrupts
- STOP Mode, can be woken up by INT0 to 15, Base Timer, TK, and CMP

2.1 Flash

Application program ROM (APROM)

- Up to 512 Kbytes of APROM
- Can be rewritten up to 100,000 times
- Supports hardware read protection and encryption
- Supports hardware write protection: Provides two regions for disabling IAP (In-Application Programming) operations. Users can configure the settings through the Code Option, with the minimum setting unit being 512 bytes (one sector)

System storage area LDRM

- 4 Kbytes system storage area, factory-programmed Bootloader

SRAM

- 32 Kbytes Internal SRAM
- Supports parity check:
 - An additional 4K RAM is used for parity: SRAM data bus width is 36 bits, including 4 parity bits (one bit per byte)
 - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
 - Provides an independent SRAM parity error flag, SRAMPEIF
 - Pay attention to the initialization of the SRAM when in use.
- Supports boot from SRAM

1.5 Kbytes user storage area (generic EEPROM)

- Divided into 3 sectors of 512 bytes each
- Can be rewritten up to 100,000 times
- Data retention time is over 10 years at room temperature

96 bits Unique ID

- 96-bit Unique ID defined in the design option area

2.2 BootLoader

- Hardware method: System storage area of 4 Kbytes, factory-programmed with Bootloader
- Software method: Supports interrupt vector table remapping, enabling flexible partitioning of the APROM area for user Bootloader execution

2.3 Flash programming and emulation

- Programming methods supported: ICP / ISP / IAP
- 2-wire JTAG / SWD programming and emulation interface
- Simulation functionality is not supported in encrypted mode

2.4 Clock source

Built-in high-frequency 64 MHz oscillator (HIRC)

- Can be used as system clock source
- Default system clock frequency at power on $f_{SYS} = f_{HIRC}/2$
- After division by two, can be used as PLL clock source
- Frequency error: within (2.0 V to 5.5 V) and (-40 to 105 °C) operating conditions, does not exceed $\pm 1\%$
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

Built-in low-frequency 37 kHz oscillator (LIRC)

- Can be used as system clock source
- Fixed as the WDT clock source, automatically enabled when WDT is enabled
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Frequency error: Within the voltage range of 2.0 to 5.5 V and at normal temperature of 25°C application environment, the frequency error after register correction does not exceed $\pm 4\%$

External 2 to 16 MHz crystal oscillator (HXT)

- Can be used as system clock source
- Can be used as a PLL clock source.
- The user can select an external Crystal Oscillator frequency below 12 MHz or equal to or above 12 MHz.

External 32.768 kHz crystal oscillator (LXT)

- Can be used as system clock source
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Supports external 32.768 kHz Oscillator
- Automatic calibration of HIRC can be performed using LXT

PLL

- Can be used as system clock source
- PLL clock source can select HIRC/2 or HXT
- PLLRCLK:
 - Maximum output frequency up to 96 MHz when used as application output
 - Maximum output frequency up to 72 MHz when used as system clock source
- PLLQCLK:
 - Output frequency is twice PLLRCLK, up to 192 MHz
 - Can serve as PWM0 clock source

2.5 Interrupt sources

- Provides 25 interrupt sources
- Four interrupt priority levels supported
- External interrupt INT
 - 16 INT interrupt sources sharing 4 interrupt vectors
 - INT signals can be remapped to all GPIO pins after configuration
 - All interrupts can be set as rising edge, falling edge, or both-edge interrupts, each with an independent corresponding interrupt flag
 - Setting the corresponding interrupt flag in software triggers entry into the corresponding interrupt

2.6 Digital peripherals

Up to 60 independent bidirectional GPIOs

- Independent pull-up resistor configuration is available
- Drive Capability of the COM port can reach 100 mA@0.8 V
- Drive Capability of the conventional port can reach 55 mA@0.8 V

Watchdog timer (WDT)

- Built-in watchdog timer (WDT) with adjustable timeout from 3.94 to 500 ms

Base timer (BTM)

- Selectable clock sources: LXT and LIRC
- Interrupt frequency interval 15.625 ms to 32 s
- Supports wake-up from STOP mode

8 16-bit timers/counters (TIM0 to TIM7)

- 16-bit up, down, and up/down auto-reload counters
- Supports rising and falling edge capture for PWM duty cycle and period measurement
- Each TIM provides two synchronized PWM outputs (TPWMA / TPWMB) with adjustable duty cycle
- Timer overflow and capture events of TIM1, TIM2, and TIM6 can trigger DMA requests
- Tn, TnCAP, and TnPWMA pins of TIM2 to TIM7 support remapping

8 16-bit advanced PWM channels

- Clock source selectable to PLLQCLK at 192 MHz
- Shared period with independently adjustable duty cycle
- Dead time insertion with complementary PWM outputs
- Supports center-aligned mode

- Supports fault detection

6 independent UART ports: UART0 to UART5

- UART0 to UART5 support signal port remapping and can be mapped to an alternate IO group
- Independent Baud Rate Generator
- Supports Wake-up from STOP Mode
- Three Communication Modes Available:
 - Mode 0, 8-bit half-duplex synchronous communication
 - Mode 1, 10-bit full-duplex asynchronous communication
 - Mode 3, 11-bit full-duplex asynchronous communication
- UART0 and UART1 support DMA request
- UART2 to 5 Do Not support DMA request

2 advanced two in one interface QSPI0/1 & SPI0/1 & TWI0/1

- QSPI0/1
 - QSPI supports Master Mode Only
 - Each QSPI supports four transfer widths: 8/16/24/32 bits
 - Fixed 8-Level FIFO with Independent TX and RX at different transfer widths
 - Supports Single-, Dual-, and Quad-Wire Communication
 - Supports two functional modes: QSPI half-duplex communication mode and pass-through mode
 - Communication speed up to 32 Mbps
 - Both QSPI interfaces can bypass FIFO for direct pass-through
 - QSPI0 and QSPI1 support DMA transfers
- SPI0/1
 - Each SPI supports four transfer widths: 8, 16, 24, and 32 bits
 - Fixed 8-level FIFO per transfer width, with separate TX and RX
 - Drive capability of signal pins enhanced in SPI mode
 - Supports Master and Slave Mode
 - SPI0 and SPI1 support DMA
- TWI0/1
 - Supports Master and Slave Mode
 - Clock stretching supported in Slave Mode
 - Communication rate up to 1 Mbps
 - Supports fast charging to ensure TWI operation at higher communication rates
 - Both TWI0 and TWI1 support DMA

2 general two in one interface SPI2/3 & TWI2/3

- SPI2/3
 - Signal ports can be mapped to 3 additional set of ports
 - Supports Master and Slave Mode
 - SPI2 supports DMA
 - SPI3 does not support DMA
- TWI2/3
 - Signal ports can be mapped to 3 additional set of ports
 - Supports Master and Slave Mode
 - Clock stretching supported in Slave Mode
 - Communication rate up to 1 Mbps
 - Supports fast charging to ensure TWI operation at higher communication rates
 - TWI2 supports DMA
 - TWI3 does not support DMA

CAN communication port

- Protocol Support:
 - CAN 2.0B
 - CAN FD
- Standby Mode supported
- Time-Stamping:
 - CiA 603: 64-bit time-stamp; Transmit frames (TTS) support a single time stamp stored in a register, whereas all Receive frames (RTS) have individual time stamps
- Transmit and Receive Buffers
 - The message buffer area is located in the SRAM, and the address can be configured

- 8 Receive Buffers (RB)
- 9 Transmit Buffers (TB)
- 8 Receive Filters (supports 29-bit ID)

Built-in CRC verification module

- Initial value is configurable, default is 0xFFFF_FFFF
- Polynomial is programmable, default is 0x04C1_1DB7
- Supports 8/16/32-bit data units

LCD/LED driving

- Selectable clock sources: LXT and LIRC
- LCD or LED selectable, sharing registers and ports
- LED
 - 8 × 31, 6 × 33, 5 × 34, or 4 × 35 segment LED driving
- LCD
 - 8 × 31, 6 × 33, 5 × 34, or 4 × 35 segment LCD driving
 - Selectable voltage division resistor values for LCD voltage output port
 - Two selectable bias voltages: 1/3 and 1/4
 - Waveform Mode: Type A and Type B selectable
 - Three selectable frame frequencies:
 - ◆ 32/64/128 Hz in Type A mode
 - ◆ 64/128/256 Hz in Type B mode

DMA

- Four independently configurable channels
- Each DMA channel can transmit DMA requests to other channels
- Data width supports Byte, Half-word, and Word
- 24 DMA request sources and four request priorities
- Supports source and target Address Auto-increment or fixed
- Supports single and burst transfer modes
- Transfer modes supported: Memory to Memory, Memory to Peripheral, Peripheral to Memory, and Peripheral to Peripheral

2.7 Analog peripherals

42-channel high sensitivity touch circuit (TK)

- **Only supported by the SC32F11T series**
- Channels can be scanned in parallel
- CMOD pin requires a 103 capacitor connected to ground
- Supports self-capacitance and mutual-capacitance modes

- TK's internal reference voltage can be set up to 4 V at the highest level to achieve higher sensitivity
- Supports low power mode
- Supports fast wake up from STOP Mode
- Suitable for capacitive proximity keys, proximity sensing, and other touch applications requiring high sensitivity
- Complete development support: highly flexible touch software library and intelligent debug software

Analog-to-digital converter (ADC)

- Precision: 14-bit
- Supports up to 20 Channels
 - External 18 ADC Sampling Channels multiplexed with other IO Port functions
 - One Internal ADC Channel can directly measure V_{DD} Voltage
 - One Internal ADC Channel can directly measure OP output
- There are four choices for the ADC reference voltage: V_{DD} and internal voltages of 2.048 V, 1.024 V, or 2.4 V
- ADC Conversion Completion Interrupt can be enabled
- Supports Single Channel Continuous Conversion Mode
- Supports DMA

Operational amplifier (OP)

- One Rail-to-Rail operational amplifier
- Configurable as PGA Mode
 - Non-inverting Input Gain: 8/16/32/64
 - Inverting Input Gain: 7/15/31/63
- Non-inverting Input routed to two external Pins: OP_P0 or OP_P1
- Inverting Input routed to one external Pin: OP_N
- An external pin is output at the output terminal: OP_O
- Output can be directly connected to ADC input
- Output can be directly connected to CMP positive pin

Analog comparator (CMP)

- Positive input signal selectable from five options:
 - Four analog signal positive input pins CMP0 to CMP3
 - OP output terminal
- Negative input voltage can be selected from the CMPR pin or one of the 15 internal V_{DD} voltage division comparison voltages
- CMP Interrupts can wake up STOP Mode

Product peripheral resource table

Peripheral Model	SC32F11T_ SC32F11G_											
	_R9	_C9	_S9	_K9	_R8	_C8	_S8	_K8	_R7	_C7	_S7	_K7
GPIOs	60	46	42	30	60	46	42	30	60	46	42	30
APROM(K byte)	512				256				128			
SRAM(Kbyte)	32											
TK	SC32F11T_(with TK)& SC32F11G_(without TK)											
QSPI	2											
SPI	4											
TWI	4											
UART	6											
CAN	1											
TIM	8											
PWM0	8	8	8	5	8	8	8	5	8	8	8	5
OP	1											
CMP	1											
ADC Channels	20	16	14	10	20	16	14	10	20	16	14	10
LCD/LED COM X SEG	8X31 6X33 5X34 4X35	8X24 6X26 5X27 4X28	7X22 5X24 4X25 3X26	4X16 2X18 1X19	8X31 6X33 5X34 4X35	8X24 6X26 5X27 4X28	7X22 5X24 4X25 3X26	4X16 2X18 1X19	8X31 6X33 5X34 4X35	8X24 6X26 5X27 4X28	7X22 5X24 4X25 3X26	4X16 2X18 1X19
CRC	YES											
DMA	YES											
Max. CPU frequency	72 MHz											

Product naming rules

	SC	32	F	1	1	T	R	9	P	J	R																																																												
Company Name	SinOne																																																																						
Device family	8=8bit 32=32bit																																																																						
Device type	A=Automotive F/G=General L=Ultra-low power H=High performance W=Wireless																																																																						
CPU core	0= Cortex-M0 1= Cortex-M0+ 2= Cortex-M3 3= Cortex-M4 4= Cortex-M7 5= Cortex-M23 6= Cortex-M33																																																																						
Subseries1	0-9																																																																						
Subseries2	T=TK G=GP M=Motor																																																																						
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Label	0	1	2	3	4	5	6	7	8	9	A	B	C	D																																																									
Size (KB)	1	2	4	8	16	32	64	128	256	512	1024	2048	-	-																																																									
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Temperature range	I= -40°C~85°C Industrial J= -40°C~105°C Automotive G2 A= -40°C~125°C Automotive G1 T= -40°C~150°C Automotive G0																																																																						
Pack type	R Tray T Tape and Reel U Tube B Bulk																																																																						

Ordering information

Model	Package	Packaging
SC32F11TR9PJR	LQFP64	Tray
SC32F11TR8PJR	LQFP64	Tray
SC32F11TR7PJR	LQFP64	Tray
SC32F11GR9PJR	LQFP64	Tray
SC32F11GR8PJR	LQFP64	Tray
SC32F11GR7PJR	LQFP64	Tray
SC32F11TC9PJR	LQFP48	Tray
SC32F11TC8PJR	LQFP48	Tray
SC32F11T/C7PJR	LQFP48	Tray
SC32F11GC9PJR	LQFP48	Tray
SC32F11GC8PJR	LQFP48	Tray
SC32F11GC7PJR	LQFP48	Tray
SC32F11TC9QJR	QFN48(0505)	Tray
SC32F11TC8QJR	QFN48(0505)	Tray
SC32F11TC7QJR	QFN48(0505)	Tray
SC32F11GC9QJR	QFN48(0505)	Tray
SC32F11GC8QJR	QFN48(0505)	Tray
SC32F11GC7QJR	QFN48(0505)	Tray
SC32F11TS9PJR	LQFP44	Tray
SC32F11TS8PJR	LQFP44	Tray
SC32F11TS7PJR	LQFP44	Tray
SC32F11GS9PJR	LQFP44	Tray
SC32F11GS8PJR	LQFP44	Tray
SC32F11GS7PJR	LQFP44	Tray
SC32F11TK9PJR	LQFP32	Tray
SC32F11TK8PJR	LQFP32	Tray
SC32F11TK7PJR	LQFP32	Tray
SC32F11GK9PJR	LQFP32	Tray
SC32F11GK8PJR	LQFP32	Tray
SC32F11GK7PJR	LQFP32	Tray
SC32F11TK9QJT	QFN32(0404)	Tape and Reel
SC32F11TK8QJT	QFN32(0404)	Tape and Reel

Model	Package	Packaging
SC32F11TK7QJT	QFN32(0404)	Tape and Reel
SC32F11GK9QJT	QFN32(0404)	Tape and Reel
SC32F11GK8QJT	QFN32(0404)	Tape and Reel
SC32F11GK7QJT	QFN32(0404)	Tape and Reel

Note: For the mass production status of specific models, please consult SinOne or the dealer's sales staff regarding sample submission and delivery times before development.

Content

1	General description.....	1
2	Features.....	2
2.1	Flash	2
2.2	BootLoader	2
2.3	Flash programming and emulation.....	2
2.4	Clock source.....	2
2.5	Interrupt sources.....	3
2.6	Digital peripherals.....	3
2.7	Analog peripherals.....	4
	Product peripheral resource table.....	5
	Product naming rules	6
	Ordering information	7
	Content.....	9
3	Pin description	14
3.1	Pin configuration.....	14
3.2	Pin resource list	18
4	Resource diagram	21
5	Flash	22
5.1	Overview.....	22
5.2	Storage block diagram.....	22
5.3	Feature	23
5.4	APROM (application program ROM).....	23
5.5	1.5 Kbytes user storage area (generic EEPROM)	25
5.6	4 Kbytes LDROM (system storage area)	25
5.6.1	BootLoader.....	26
5.7	SRAM	26
5.8	Boot area selection (bootstrap)	26
5.8.1	Bootstrap from application program ROM	26
5.8.2	Bootstrap from system memory	27
5.8.3	Bootstrapping from embedded SRAM	27
5.8.4	Bootstrap mode configuration	27
5.8.5	96 bits Unique ID.....	27
5.9	User ID area	27
5.10	Programming	27
5.11	JTAG specific mode.....	28
5.12	Normal mode (JTAG specific pins disabled)	28
5.13	Security encryption	29
5.13.1	Security encryption access rights	29

5.14	In application programming (IAP).....	29
5.14.1	IAP operation related registers.....	30
5.15	Option byte area (Customer Option)	32
5.15.1	Mapping register for Customer Option	32
6	Power, reset and system clock (RCC).....	35
6.1	Power-on process.....	35
6.1.1	Reset stage	35
6.1.2	Loading information stage.....	35
6.1.3	Normal operation stage.....	35
6.2	Reset	35
6.2.1	Hardware reset.....	36
6.2.2	Software reset	37
6.2.3	Boot area after reset	37
6.2.4	Initial reset state	37
6.3	Clock.....	37
6.3.1	System clock source	37
6.3.2	Built-in high-frequency 64 MHz oscillator (HIRC)	38
6.3.3	Built-in high-frequency crystal oscillator circuit, can be externally connected to a 2 to 16 MHz high-frequency oscillator (HXT)	38
6.3.4	Built-in low-frequency 37 kHz oscillator (LIRC)	38
6.3.5	Built-in low frequency oscillator circuit, with support for external 32.768 kHz low frequency oscillator (LXT).....	39
6.3.6	PLL	39
6.4	Register access clock and peripheral clock source	40
6.4.1	Register access clock	40
6.4.2	Peripheral clock source.....	40
6.4.3	Bus clock.....	40
6.4.4	Peripheral clock.....	42
6.4.5	Peripheral clock block diagram	43
6.4.6	Peripheral clock enable register.....	43
6.4.7	Low-power mode clock	43
6.5	RCC interrupt.....	43
7	Interrupts.....	45
7.1	External interrupts INT0 to INT15.....	45
7.2	Interrupt and events.....	45
7.3	Interrupt vector table.....	46
8	Power saving mode	50
9	GPIO	51
9.1	Clock source.....	51
9.2	Feature	51
9.3	GPIO block diagram	51

9.3.1	Strong push-pull output mode	51
9.3.2	Input mode with pull-up	52
9.3.3	High impedance input mode (input only)	52
10	Analog-to-digital converter (ADC).....	53
10.1	Clock source	53
10.2	Feature	53
10.3	ADC conversion steps	53
10.4	ADC interrupts	54
10.5	ADC connection circuit diagram	54
11	Operational amplifier and programmable gain amplifier (OP)	55
11.1	Feature	55
11.2	OP port selection	55
11.2.1	OP non-inverting input selection	55
11.2.2	OP inverting input selection	55
11.2.3	OP output selection	55
11.3	Block diagram of the OP circuit structure	56
12	Analog comparator (CMP)	57
12.1	Feature	57
12.2	Analog comparator block diagram.....	57
13	UART0 to 5	58
13.1	Clock source	58
13.2	Feature	58
14	QSPI0 to 1	59
14.1	Clock source	59
14.2	QSPI0/1 feature	59
15	SPI0 to 3	60
15.1	Clock source	60
15.2	SPI0/1 feature.....	60
15.3	SPI2/3 features.....	60
15.4	Comparison between SPI0/1 and SPI2/3.....	61
16	TWI0 to 3	62
16.1	Clock source	62
16.2	TWI0/1 features	62
16.3	Features of TWI2 and TWI3	62
16.4	TWI signal description	62
17	CAN communication port.....	64
17.1	Overview	64
17.2	Clock source	64
17.3	Feature	64
18	Hardware watchdog WDT	65
18.1	Clock source	65

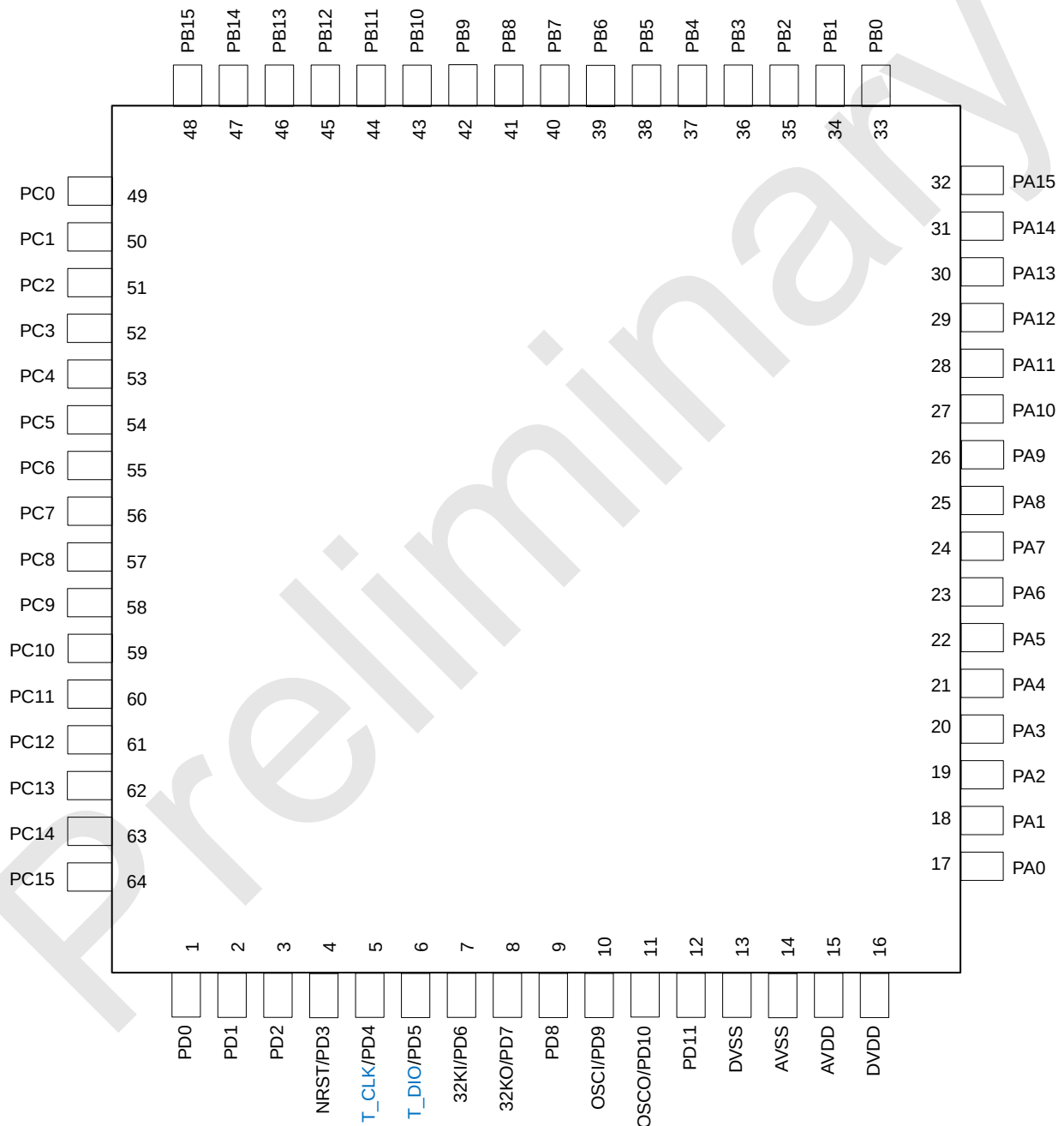
19	Base timer (BTM).....	66
19.1	Clock source	66
19.2	Feature	66
20	Built-in CRC verification module.....	67
20.1	Clock source.....	67
20.2	Feature	67
21	PWM0: 8-channel 16-bit multifunction PWM.....	68
21.1	Clock source.....	68
21.2	Feature	68
21.3	PWM0 block diagram	69
21.4	PWM0 general configuration	69
21.4.1	Output mode	69
21.4.2	Alignment type	70
21.4.3	Duty cycle variation feature.....	70
21.4.4	Period change feature.....	70
22	LCD/LED driver.....	71
22.1	Clock source.....	71
22.2	Built-in 8 COM x 31 SEG LED driver.....	71
22.3	Built-in 8 COM x 31 SEG LCD driver	71
23	42-channel high sensitivity touch circuit (TK).....	72
24	16-bit timers/counters (TIM) Timer0 to Timer7	73
24.1	Clock source.....	73
24.2	Feature	73
24.3	Counting method	73
24.3.1	TIM counting method in timer mode	73
24.3.2	TIM counting method in PWM output mode	73
24.4	Timer-related signal pins	73
24.5	TIM interrupts and their corresponding flags.....	74
24.6	TIM operating modes.....	74
25	DMA controller	75
25.1	Overview.....	75
25.2	Clock source.....	75
25.3	Feature	75
25.4	Function description	75
25.4.1	Transfer direction	75
25.4.2	DMA access region restriction	75
25.4.3	Channel priority	75
25.4.4	Single transfer and burst transfer.....	76
25.5	Loop mode.....	76
26	Systick.....	77
26.1	Clock source.....	77

26.2	Systick calibration register default value	77
27	Electrical characteristics	78
27.1	Recommended operating conditions	78
27.2	Absolute maximum ratings	78
27.3	Flash ROM parameters	78
27.4	Power consumption	79
27.4.1	$V_{DD} = 5\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$, booting from APROM unless otherwise specified	79
27.4.2	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$, boot from APROM unless otherwise specified	79
27.5	GPIO parameter	79
27.5.1	$V_{DD} = 5\text{ V}$; $T_A = +25\text{ }^{\circ}\text{C}$, unless otherwise specified	79
27.5.2	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$, unless otherwise specified	80
27.6	TK electrical characteristics	81
27.7	BTM electrical characteristics	81
27.8	WDT electrical characteristics	81
27.9	AC electrical characteristics	82
27.10	ADC electrical characteristics	82
27.11	CMP electrical characteristics	83
27.12	OP electrical parameters	83
28	Package information	85
29	Revision history	95
30	Important notice	96

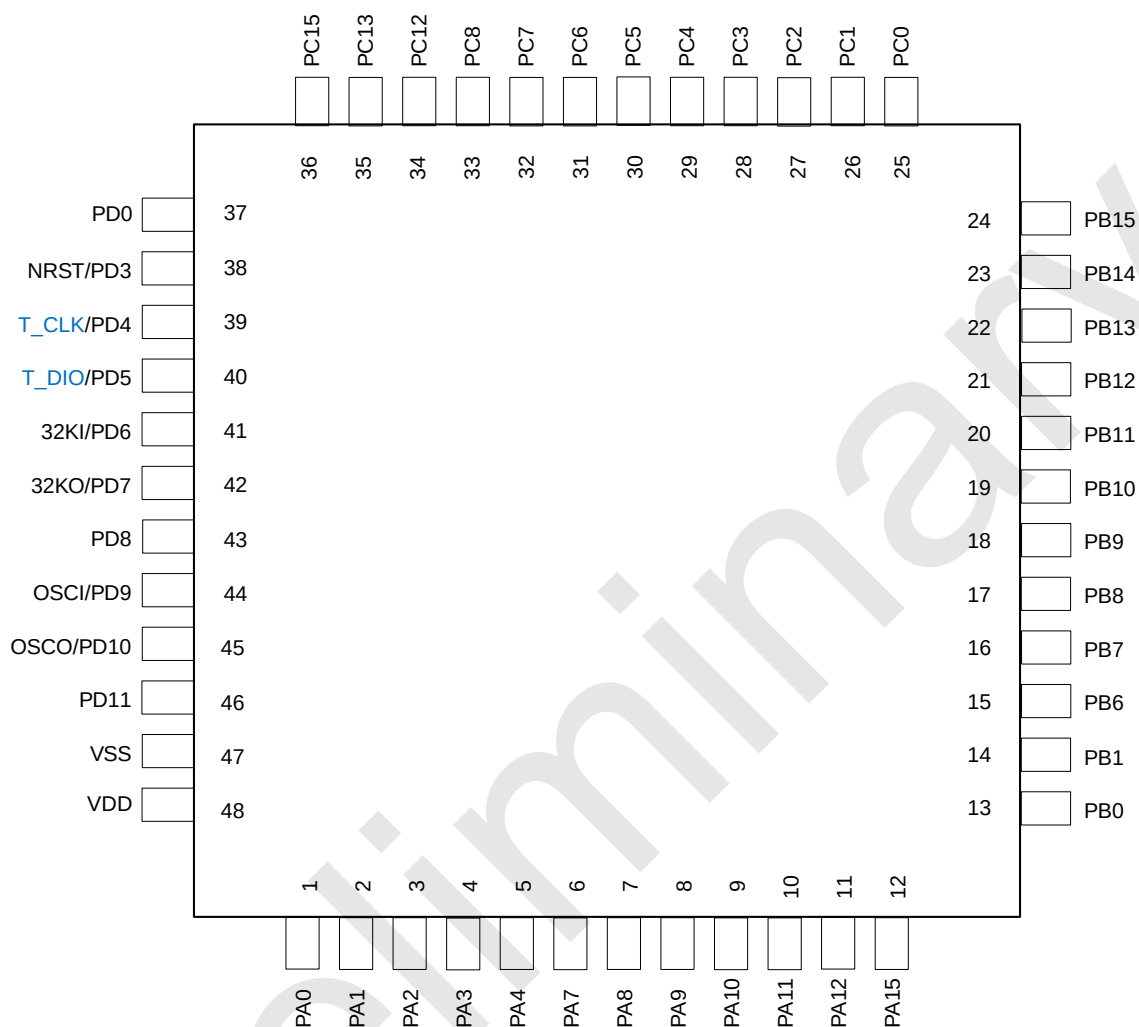
3 Pin description

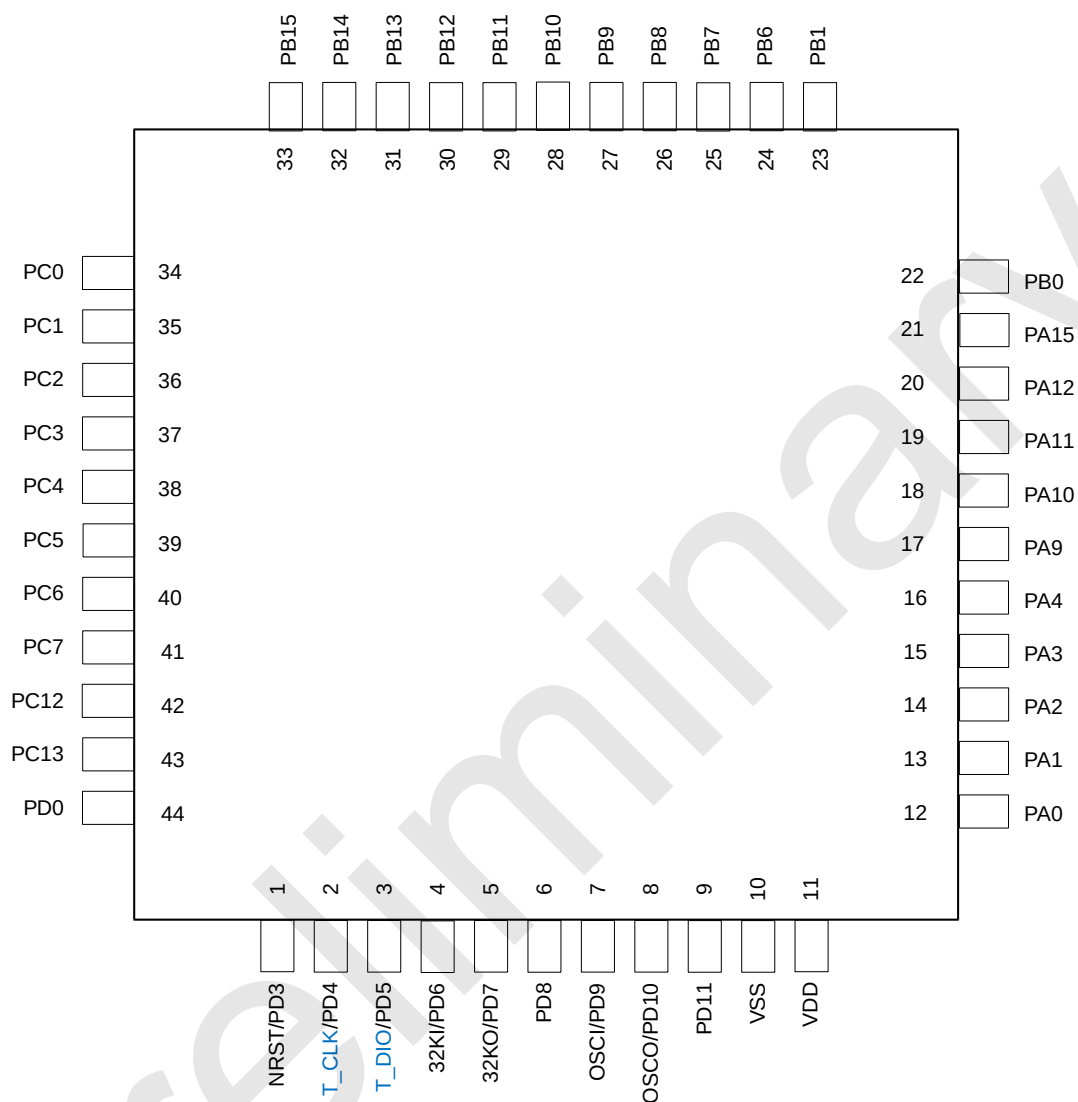
3.1 Pin configuration

Note: Only the SC32F11T series supports the TK function.

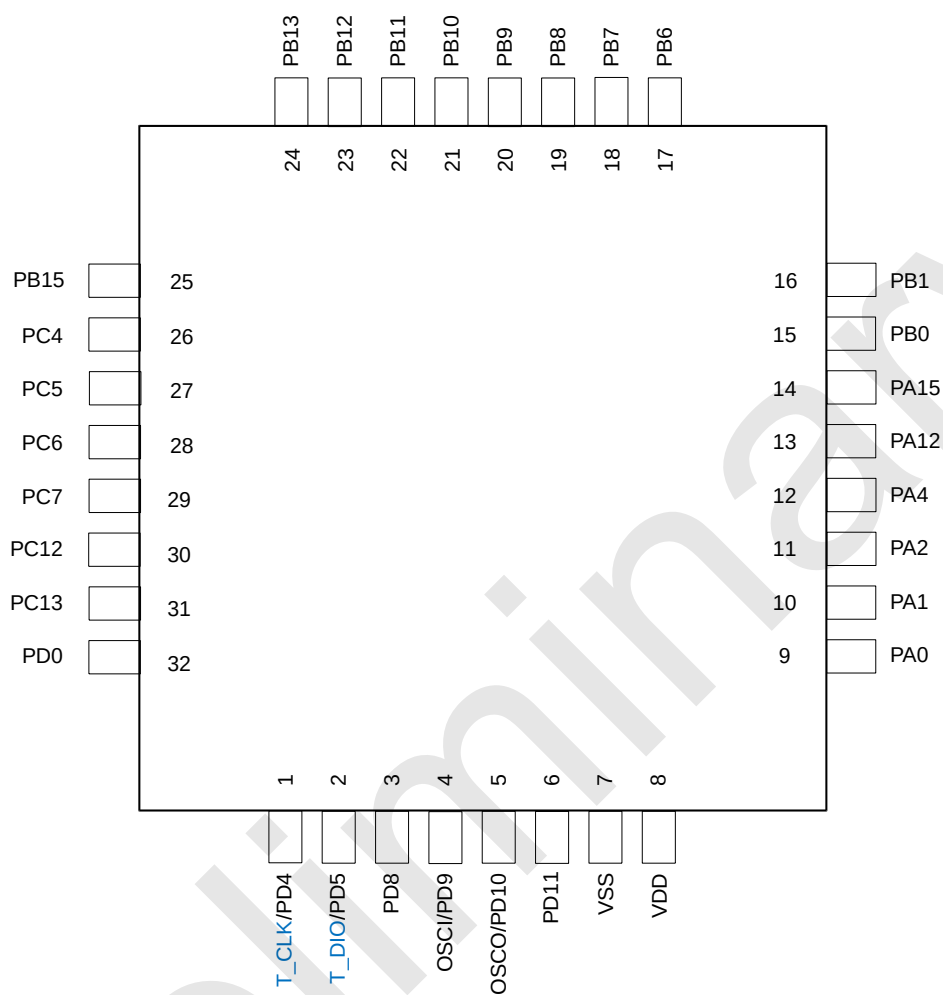


64PIN Pin Configuration
For LQFP64 Package





44PIN Pin Configuration
For LQFP44 Package



32PIN Pin Configuration
For LQFP32 and QFN32 Packages

3.2 Pin resource list

Note: Only the SC32F11T series supports the TK function.

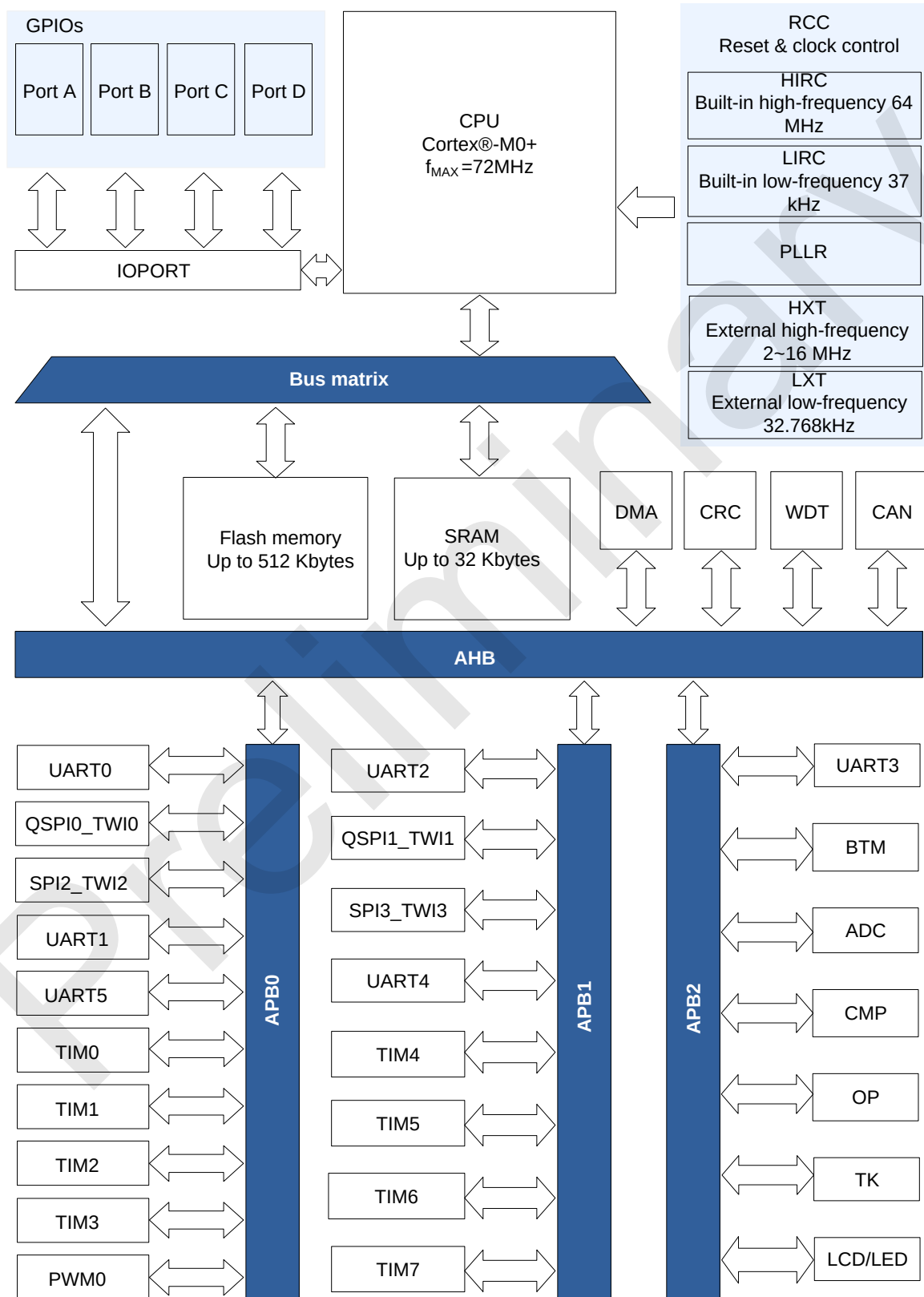
LQFP32	LQFP44	LQFP48/QFN48	LQFP64	Pin Name	Special	TK	LCD/LED	ADC/PGA	CMP/PGA	OP	PWM-8	UART	QSPI	SPI	TWI	TPWM	TIM	CAN	INT
32	44	37	1	PD0	-	TK28	S33	AN15	-	-	-	-	-	-	-	-	-	-	INT00
-	-	-	2	PD1	-	-	-	-	-	-	-	-	-	-	-	T4PWMB	T4EX	-	INT01
-	-	-	3	PD2	-	-	-	-	-	-	-	-	-	-	-	T4PWMA	T4CAP/T4	-	INT02
-	1	38	4	PD3	NRST	TK29	S34	-	-	-	-	-	-	-	-	T7PWMA	T7CAP/T7	-	INT03
1	2	39	5	PD4	T_CLK	-	-	-	-	-	-	RXD1	-	-	-	T7PWMB	T7EX	-	INT04
2	3	40	6	PD5	T_DIO	-	-	-	-	-	-	TXD1	-	-	-	-	-	-	INT05
-	4	41	7	PD6	32KI	-	-	-	-	-	-	-	-	-	-	-	-	-	INT06
-	5	42	8	PD7	32KO	-	-	-	-	-	-	-	-	-	-	-	-	-	INT07
3	6	43	9	PD8	-	-	-	AN16	-	-	PWM3	-	-	-	-	-	-	-	INT08
4	7	44	10	PD9	OSCI	-	-	-	-	-	PWM2	-	-	-	-	-	-	-	INT09
5	8	45	11	PD10	OSCO	-	-	-	-	-	PWM1	-	-	-	-	-	-	-	INT10
6	9	46	12	PD11	-	CMOD	-	AN17	-	-	PWM0	-	-	-	-	-	-	-	INT11
7	10	47	13	VSS/DVSS ¹	Power	-	-	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	14	VSS/AVSS ¹	Power	-	-	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	15	VDD/AVDD ¹	Power	-	-	-	-	-	-	-	-	-	-	-	-	-	
8	11	48	16	VDD/DVDD ¹	Power	-	-	-	-	-	-	-	-	-	-	-	-	-	
9	12	1	17	PA0	-	-	-	-	CMPR	-	-	RXD5	-	SCK2	SCL2	-	-	-	INT00
10	13	2	18	PA1	-	-	-	-	CMP3	OP_N	-	TXD5	-	MOSI2	SDA2	-	-	-	INT01
11	14	3	19	PA2	-	TK30	-	-	CMP2	OP_P0	-	(TXD0)	-	MISO2/SCK3	SCL3	-	-	-	INT02
-	15	4	20	PA3	-	TK31	-	-	CMP1	OP_P1	-	(RXD0)	-	MOSI3	SDA3	-	-	-	INT03
12	16	5	21	PA4	-	TK32	-	-	CMP0	OP_O	-	-	-	MISO3	-	T3PWMA	T3CAP/T3	-	INT04
-	-	-	22	PA5	-	TK33	-	-	-	-	-	(TXD2)	-	-	-	-	-	-	INT05
-	-	-	23	PA6	-	TK34	-	-	-	-	-	(RXD2)	-	-	-	-	-	-	INT06
-	-	6	24	PA7	-	TK35	-	-	-	-	-	-	-	(SCK3A)	(SCL3A)	-	-	-	INT07
-	-	7	25	PA8	-	TK36	C7	-	-	-	-	-	-	(MOSI3A)	(SDA3A)	-	-	-	INT08
-	17	8	26	PA9	-	TK37	C6	-	-	-	PWM4	-	-	(MISO3A)	-	-	-	-	INT09

LQFP32	LQFP44	LQFP48/QFN48	LQFP64	Pin Name	Special	TK	LCD/LED	ADC/PGA	CMP/PGA	OP	PWM-8	UART	QSPI	SPI	TWI	TPWM	TIM	CAN	INT
-	18	9	27	PA10	-	TK38	C5	-	-	-	PWM5	-	-	(MISO2A)	-	-	-	-	INT10
-	19	10	28	PA11	-	TK39	C4	-	-	-	PWM6	-	-	(MOSI2A)	(SDA2A)	-	-	-	INT11
13	20	11	29	PA12	-	TK40	C3/S0	-	-	-	PWM7	-	-	(SCK2A)	(SCL2A)	T6PWMB	T6EX	-	INT12
-	-	-	30	PA13	-	TK41	-	-	-	-	-	(RXD5)	-	-	-	T6PWMA	T6CAP/T6	-	INT13
-	-	-	31	PA14	-	TK0	-	-	-	-	-	(TXD5)	-	-	-	T5PWMA	T5CAP/T5	-	INT14
14	21	12	32	PA15	-	TK1	C2/S1	-	-	-	-	-	QSPI1CLK	SCK1	SCL1	T5PWMB	T5EX	-	INT15
15	22	13	33	PB0	-	TK2	C1/S2	-	-	-	-	-	QSPI1IO0	MOSI1	SDA1	-	-	-	INT00
16	23	14	34	PB1	-	TK3	C0/S3	-	-	-	-	-	QSPI1IO1	MISO1	-	-	-	-	INT01
-	-	-	35	PB2	-	-	S4	-	-	-	-	-	-	-	-	-	-	-	INT02
-	-	-	36	PB3	-	-	S5	-	-	-	-	-	-	-	-	-	-	-	INT03
-	-	-	37	PB4	-	-	S6	-	-	-	-	-	-	-	-	-	-	-	INT04
-	-	-	38	PB5	-	-	S7	-	-	-	-	-	-	(SCK3B)	(SCL3B)	T3PWMB	T3EX	-	INT05
17	24	15	39	PB6	-	TK4	S8	-	-	-	-	TXD4	QSPI1IO2	(MOSI3B)	(SDA3B)	T2PWMA	T2CAP/T2	-	INT06
18	25	16	40	PB7	-	TK5	S9	-	-	-	-	RXD4	QSPI1IO3	(MISO3B)	-	T1PWMA	T1CAP/T1	-	INT07
19	26	17	41	PB8	-	TK6	S10	-	-	-	-	-	QSPI0CLK	SCK0	SCL0	(T2PWMA A)	(T2CAP A/T2 A)	-	INT08
20	27	18	42	PB9	-	TK7	S11	-	-	-	-	RXD2	QSPI0IO0	MOSI0/(SCK2B)	SDA0/(SCL2B)	(T3PWMA A)	(T3CAP A/T3 A)	-	INT09
21	28	19	43	PB10	-	TK8	S12	-	-	-	-	TXD2	QSPI0IO1	MSIO0/(MOSI2B)	(SDA2B)	(T4PWMA A)	(T4CAP A/T4 A)	-	INT10
22	29	20	44	PB11	-	TK9	S13	-	-	-	-	TXD0	QSPI0IO2	(MISO2B)/(MISO3C)	-	(T5PWMA A)	(T5CAP A/T5 A)	-	INT11
23	30	21	45	PB12	-	TK10	S14	-	-	-	-	RXD0	QSPI0IO3	(MOSI3C)	(SDA3C)	(T6PWMA A)	(T6CAP A/T6 A)	-	INT12
24	31	22	46	PB13	-	TK11	S15	-	-	-	FLT	-	-	(SCK3C)	(SCL3C)	(T7PWMA A)	(T7CAP A/T7 A)	-	INT13
-	32	23	47	PB14	-	TK12	S16	-	-	-	-	-	-	-	-	-	-	-	INT14
25	33	24	48	PB15	-	TK13	S17	ANI0	-	-	-	-	-	-	-	-	-	-	INT15
-	34	25	49	PC0	-	TK14	S18	ANI1	-	-	-	-	-	-	-	-	-	-	INT00
-	35	26	50	PC1	-	TK15	S19	ANI2	-	-	-	-	-	-	-	-	-	-	INT01
-	36	27	51	PC2	-	TK16	S20	ANI3	-	-	-	-	-	-	-	-	-	-	INT02
-	37	28	52	PC3	-	TK17	S21	ANI4	-	-	-	(RXD4)	-	-	-	-	-	-	INT03
26	38	29	53	PC4	-	TK18	S22	ANI5	-	-	-	(TXD4)	-	-	-	-	-	-	INT04
27	39	30	54	PC5	-	TK19	S23	ANI6	-	-	-	(RXD3)	-	-	-	-	-	-	INT05
28	40	31	55	PC6	-	TK20	S24	ANI7	-	-	-	(TXD3)	-	-	-	-	-	CAN_RX	INT06
29	41	32	56	PC7	-	TK21	S25	ANI8	-	-	-	-	-	-	-	-	-	CAN_TX	INT07

LQFP32	LQFP44	LQFP48/QFN48	LQFP64	Pin Name	Special	TK	LCD/LED	ADC/PGA	CMP/PGA	OP	PWM-8	UART	QSPI	SPI	TWI	TPWM	TIM	CAN	INT
-	-	33	57	PC8	-	TK22	S26	ANI9	-	-	-	-	-	-	-	-	-	-	INT08
-	-	-	58	PC9	-	-	S27	ANI10	-	-	-	-	-	(SCK2C)	(SCL2C)	-	-	-	INT09
-	-	-	59	PC10	-	TK23	S28	ANI11	-	-	-	(RXD1)	-	(MOSI2C)	(SDA2C)	-	-	-	INT10
-	-	-	60	PC11	-	TK24	S29	ANI12	-	-	-	(TXD1)	-	(MISO2C)	-	-	-	-	INT11
30	42	34	61	PC12	-	TK25	S30	-	-	-	-	RXD3	-	-	-	T2PWMB	T2EX	-	INT12
31	43	35	62	PC13	-	TK26	S31	-	-	-	-	TXD3	-	-	-	T0PWMA	T0CAP/T0	-	INT13
-	-	-	63	PC14	-	-	-	ANI13	-	-	-	-	-	-	-	T1PWMB	T1EX	-	INT14
-	-	36	64	PC15	-	TK27	S32	ANI14	-	-	-	-	-	-	-	T0PWMB	T0EX	-	INT15

Note: DVSS: Digital Ground, DVDD: Digital Power Supply; AVSS: Analog Ground, AVDD: Analog Power Supply.

4 Resource diagram

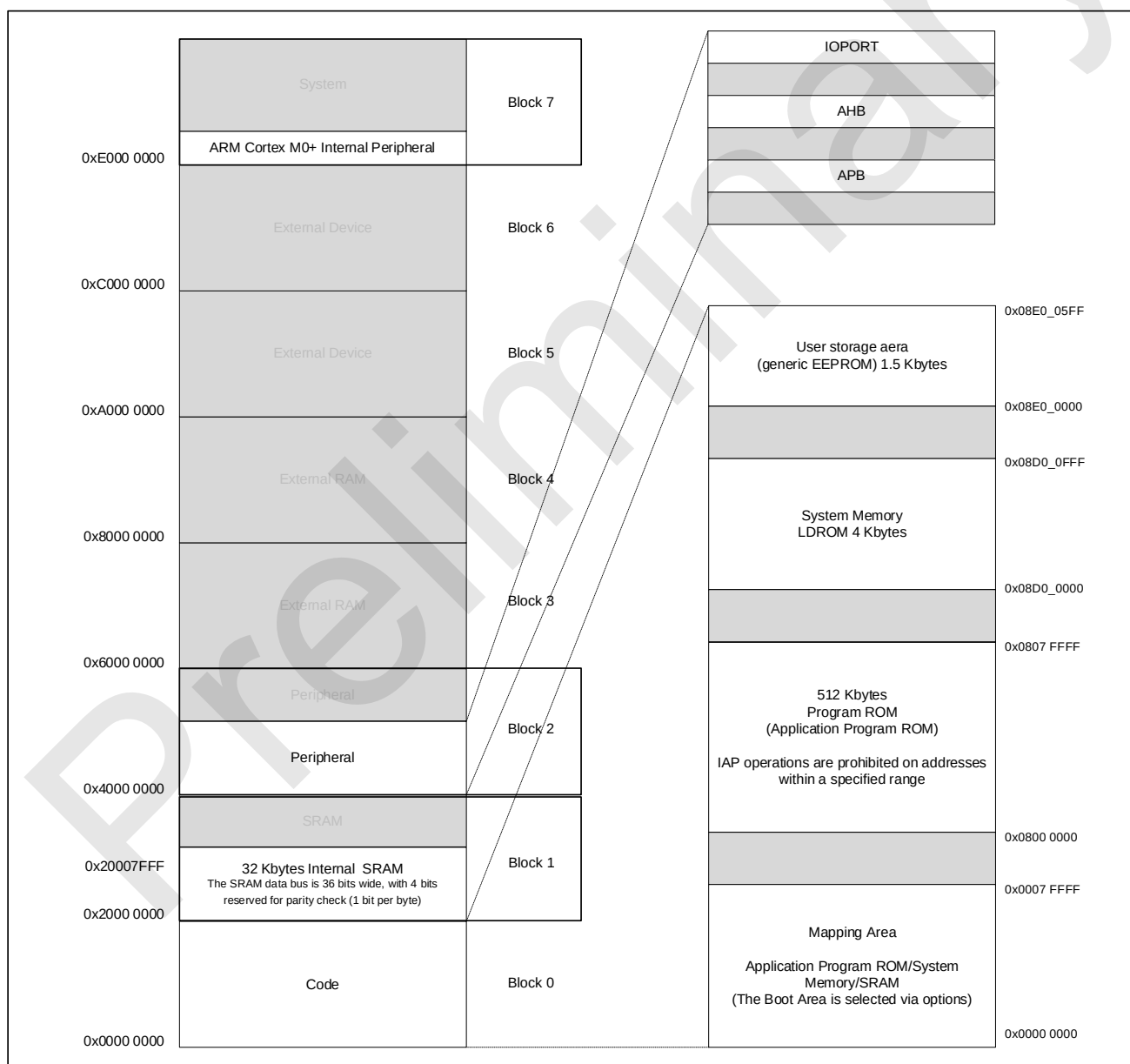


5 Flash

5.1 Overview

Program memory, data memory, and registers are arranged within the same linear (i.e., contiguous address) 4 GB address space. Bytes in memory are encoded using Little-endian Format. Within a word, the byte with the lowest number is considered the Least Significant Byte, while the byte with the highest number is considered the Most Significant Byte. The addressable Flash is divided into 8 main blocks, each block of 512 MB.

5.2 Storage block diagram



5.3 Feature

- The Flash has a 32-bit width and supports up to 100,000 write cycles.
- Data retention time at room temperature exceeds 10 years.
- The Flash memory is organized as follows:
 - Up to 512 Kbytes APROM (Application Program ROM)
 - 4 Kbytes LDROM (system storage area)
 - 1.5 Kbytes User Storage Area (Generic EEPROM)
 - 32 Kbytes Internal SRAM with Parity Check Function
 - 96 bits Unique ID.

5.4 APROM (application program ROM)

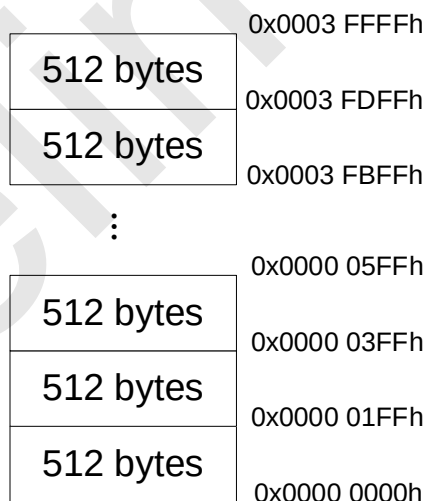
- The APROM of the SC32F11xx9 Series has 512 Kbytes
- The APROM of the SC32F11xx8 Series has 256 Kbytes
- The APROM of the SC32F11xx7 Series has 128 Kbytes
- Sector size: 512 bytes
- Support: Read/Write, Sector Erase, Chip Erase, and Blank Check
- The CPU (Cortex®-M0+) accesses Flash via the AHB Bus
- By default, the program starts from the Application Program ROM. Users can select program startup from SRAM, LDROM, or other regions through the Customer Option OP_BL[1:0]
- Read Protection (read encryption): when enabled, only programs launched from the Application Program ROM can read information from it. Programs started from other regions or third-party tools cannot access this information
- Write Protection: offers two hardware write protection Segments. IAP operation is disabled within the write protected Segments. Users can configure the size of these write protection Segments by sector based on actual requirements.

512 Kbytes Flash ROM is divided into 1024 Sectors, each Sector is 512 bytes. During programming, the Sector corresponding to the target Address will be forcibly erased by the programmer before data is written; users must erase first before writing data.



SC32F11xx9 series 512 Kbytes Flash ROM sector partition diagram

256 Kbytes APROM is divided into 512 Sectors, each Sector is 512 bytes. During programming, the Sector corresponding to the target Address will be forcibly erased by the programmer before data is written; users must erase first before writing data.



SC32F11xx8 series 256 Kbytes APROM sector partition diagram

The 128 Kbytes APROM is divided into 256 sectors, each sector being 512 bytes. During programming, the sector containing the target address will be forcibly erased by the programmer before data is written; user write operations must first erase, then write data.

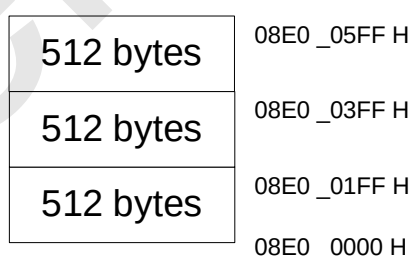


SC32F11xx7 series 128 Kbytes APROM sector partition diagram

5.5 1.5 Kbytes user storage area (generic EEPROM)

The 1.5 Kbytes independent EEPROM area is located at addresses 0x08E0_0000 H to 0x08E0_05FF H, configured by the IAPADE register. The independent EEPROM supports up to 100,000 write cycles and maintains data retention for more than 10 years at room temperature. The independent EEPROM supports Blank Check, Programming, Verification, Erase, and Read functions.

EEPROM contains 3 sectors in total, each sector is 512 bytes:



EEPROM sector partition diagram

Note: The EEPROM endurance erase/write cycles are 100,000 times. Users should not exceed the EEPROM's rated programming cycles during erase/write operations, as this may cause malfunctions!

5.6 4 Kbytes LDROM (system storage area)

- The system storage area is a 4 Kbytes LDROM, factory programmed with the ISP Program. This area is neither writable nor accessible by users.
- Users can select booting from the LDROM area via the Customer Option OP_BL[1:0].

- Embedded Bootloader Program: The factory-programmed ISP Program, which is publicly available and enables updating program Flash via UART. The program execution waits for an upgrade command. If no update command is received within 500 ms, it jumps to execute the Application Program ROM at address 0X0800 0000.

5.6.1 BootLoader

Supports both hardware and software BootLoad methods:

- Software approach: Directly divide BootLoad and APP segments via software. By modifying VTOR, BootLoad and APP interrupts can be easily shared, and each segment's size can be freely adjusted.
- Hardware approach: 4 Kbytes fixed System Memory as a dedicated BootLoader area, which users cannot read or write:
 - The Loader ROM serves as a fixed BootLoader space. The program is programmed before the production stage, and users cannot read or write it.
 - Embedded Bootloader Program: The Embedded Bootloader Program is located in System Memory and programmed during the production stage. Fixed ISP Program: This instruction is public and can be used to reprogram Flash via UART using this program.

5.7 SRAM

- Internal SRAM: 32 Kbytes, address range 0x2000 0000 to 0x2000 7FFF.
- Supports parity check:
 - An additional 4 Kbytes RAM is used for parity check: the SRAM data bus width is 36 bits, of which 4 bits are for parity check (1 bit per byte).
 - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a parity check bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
 - Provides an independent SRAM parity error flag, SRAMPEIF.

Note: When enabling SRAM parity check, it is recommended to perform software initialization of the entire SRAM at the start of the code to avoid parity check errors when reading uninitialized locations.

- Users can select program startup from SRAM by setting the Customer Option OP_BL[1:0].
- Accessible at the maximum system clock frequency by byte, half-word (16-bit), or full word (32-bit) with no wait states, enabling access by both the CPU and DMA.

5.8 Boot area selection (bootstrap)

After reset, the user can configure the required bootstrap mode.

After exiting standby mode, the startup mode configuration can be resampled. After this startup delay ends, the CPU will fetch the stack top value from address 0x0000 0000, then begin executing code from the bootstrap memory starting at 0x0000 0004.

There are three bootstrap area options: application program ROM, system storage area, and SRAM, described in detail below:

5.8.1 Bootstrap from application program ROM

The application program ROM has an alias in the bootstrap memory space (0x0000 0000), but it can also

be accessed from its original memory space (0x0800 0000). In other words, the program can start accessing memory from address 0x0000 0000 or 0x0800 0000.

5.8.2 Bootstrap from system memory

- The system memory area (4 Kbytes independent LDROM) acts as a fixed BootLoader space, with the program factory programmed and inaccessible for user read or write.
- Embedded Bootloader Program: The Embedded Bootloader Program is located in System Memory and programmed during the production stage. The embedded ISP Program is public and can be used to reprogram Flash via various Communication Interfaces (UART, TWI, and SPI).

5.8.3 Bootstrapping from embedded SRAM

SRAM has an Alias in the Bootstrap Memory space (0x0000 0000), but it can also be accessed from its original Memory space (0x2000 0000).

5.8.4 Bootstrap mode configuration

Three Bootstrap modes can be selected through the Control Bits BTLD[1:0] combined with the Software Reset (RST) Control Bit. BTLD and RST are protected by IAP_KEY:

1. Set BTLD[1:0] = 0x00; after chip software reset, boot from the Application Program ROM (APROM).
2. Set BTLD[1:0]=0x01; after chip software Reset, boot from the system storage area (LDROM).
3. Set BTLD[1:0]=0x10; after chip software Reset, boot from embedded SRAM.

The initial chip power-on boot area selection is configured via the Customer Option OP_BL[1:0]:

1. Set OP_BL[1:0]=0x00 in the Customer Option; after chip Reset, boot from the Application Program ROM (APROM).
2. Set OP_BL[1:0]=0x01 in the Customer Option; after chip Reset, boot from the system storage area (LDROM).
3. Set OP_BL[1:0]=0x10 in the Customer Option; after chip Reset, boot from embedded SRAM.

5.8.5 96 bits Unique ID

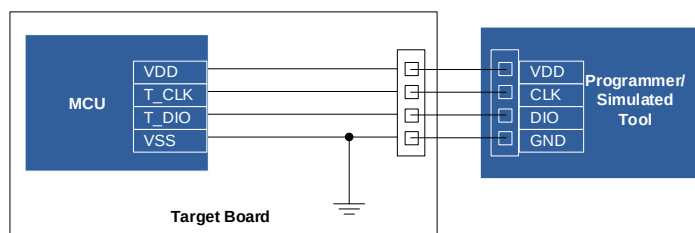
The SC32F11T/11G provides an independent Unique ID Area with a 96-bit unique code pre-programmed before shipment to ensure chip uniqueness. The only method for users to obtain the serial number is via IAP instructions.

5.9 User ID area

The User ID Area is programmed at the factory with a user-customized ID. Users may read this ID but are disabled from writing to the User ID Area.

5.10 Programming

The SC32F11T/11G Flash is programmed via T_DIO, T_CLK, VDD, and VSS, with the specific connection relationships as follows:



ICP Mode Flash Writer Programming Connection Diagram

T_DIO and T_CLK are two-wire JTAG signals for Flash Programming and Emulation. During programming, users can configure the modes of these two ports through the Customer Option: JTAG Specific Mode and Normal Mode (the JTAG Specific Port is disabled in Normal Mode).

5.11 JTAG specific mode

In JTAG Specific Mode, T_DIO and T_CLK are dedicated pins for programming and simulation, and all other functions multiplexed with them are disabled. This mode is typically used during online debugging to facilitate user simulation and debugging. Once JTAG Specific Mode is enabled, the chip can directly enter programming or simulation mode without needing to power cycle.

5.12 Normal mode (JTAG specific pins disabled)

In Normal Mode, JTAG functionality is disabled, and other functions multiplexed on the ports operate normally. This mode prevents the programming port from occupying MCU pins, enabling users to maximize MCU resource utilization.

Note: After successfully configuring to disable the JTAG specific pins, the chip must be completely powered off and then powered on again before entering programming or simulation mode. This affects programming and simulation in powered-on mode. SinOne recommends users select the configuration that disables the JTAG dedicated port during mass production programming, and choose JTAG mode during R&D debug.

The related Customer Options are listed below:

Register	Read/Write	Description	Reset Value
OPT_CON1	R/W	Customer Option Mapping Register 1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit Number	Bit Symbol	Description
6	DISJTG	JTAG Port Switching Control Bit 0: JTAG Mode Enable, corresponding pins can only be used as T_CLK/ T_DIO 1: Normal Mode, JTAG function disabled

5.13 Security encryption

The security encryption function of the SC32F11T/11G Series primarily provides read protection encryption for APROM: during programming, users configure the read protection encryption function in the Customer Option setting of the SinOne dedicated programming suite's host software, select whether to enable flash read protection, and enter encryption mode:

- By default, the chip's flash is non-encrypted at factory shipment.
- The read protection encryption function does not have a mapping register; users can only configure it in the Customer Option setting of the SinOne dedicated programming suite's host software during programming, and modifications require programming.
- Encryption disabled: read, programming, and erase operations can be performed on the Application Program ROM. All operations on option bytes and backup registers are also allowed.
- Encryption Enable:
 - Application Program ROM Bootstrap: Code running in user mode (bootstrapped from user APROM) can perform all operations on the Application Program ROM.
 - Debug, enable from SRAM and LDROM: In debug mode or when code is booted from SRAM or LDROM, APROM is completely inaccessible.
- Disabling encryption requires a full erase of the Application Program ROM first.

5.13.1 Security encryption access rights

Boot Area/Tools	Unlock State					Read Protection Encryption Status				
	Read	Write	Block Erase	Full Erase	Operate on Write Protection Area	Read	Write	Block Erase	Full Erase	Operate on Write Protection Area
Bootstrap from APROM	√	√	√	\	Disable	√	√	√	\	Disable
Debug / Bootstrap from SRAM	√	√	√	√	Disable	Disable	Disable	Disable	Disable	Disable
Bootstrap from LDROM	√	√	√	√	√	Disable	Disable	Disable	√	Disable

5.14 In application programming (IAP)

The IAP area in the APROM of SC32F11T/11G supports In Application Programming (IAP) operations, allowing users to perform remote program updates or read information from the Unique ID Area or User ID Area via IAP. Before performing IAP write operations, users must erase the sector corresponding to the target address.

By default, the chip's APROM permits global IAP operations out of the factory. The chip internally provides two flash write protection regions, configured in sector units starting at specified addresses; the protected regions prohibit IAP operations. The configuration rules are as follows:

IAPPORx Register value (x = A or B)	IAPPOR Protection Area
IAPPORx_ST = IAPPORx_ED	Sector IAPPORx
IAPPORx_ST > IAPPORx_ED	None (Unprotected)
IAPPORx_ST < IAPPORx_ED	Sectors from IAPPORx_ST to IAPPORx_ED

Users can configure these two APROM write protection segments via the 'Flash sectors protection' option in

the Customer Option during programming.

Note: IAP does not support single- or double-byte programming; IAP writes must be word-aligned (4-byte aligned).

5.14.1 IAP operation related registers

IAP operations on APROM outside the write protection area can be performed through the following registers:

5.14.1.1 Data protection register IAP_KEY

Register	Read/Write	Description	Reset Value
IAP_KEY	R/W	Data Protection Register	0x0000_0000

31	30	29	28	27	26	25	24
IAPKEY[31:24]							
23	22	21	20	19	18	17	16
IAPKEY[23:16]							
15	14	13	12	11	10	9	8
IAPKEY[15:8]							
7	6	5	4	3	2	1	0
IAPKEY[7:0]							

Bit Number	Bit Symbol	Description
31 ~ 0	IAPKEY[31:0]	Data Protection Lock To prevent accidental Flash operations caused by electrical interference or other factors, write operations to the IAP_CON Register must first be unlocked using the IAPKEY. The unlock sequence is as follows: 1. Write KEY1 = 0x1234_5678 2. Write KEY2 = 0xA05F_05FA If the sequence is incorrect, the IAP_CON Register is locked and remains so until the next System Reset.

5.14.1.2 IAP sector number setting register IAP_SNB

Register	Read/Write	Description	Reset Value
IAP_SNB	R/W	IAP Sector Number Setting Register	0x0000_0000

31	30	29	28	27	26	25	24
IAPADE[7:0]							
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	IAPSNB[8]
7	6	5	4	3	2	1	0
IAPSNB[7:0]							

Bit Number	Bit Symbol	Description
31 ~ 24	IAPADE[7:0]	IAP Operation Area Extended Address By writing different values to IAPADE, the IAP operation targets different operation areas: 0x00: Invalid

Bit Number	Bit Symbol	Description
		0x4C:APROM 0x69:EEPROM 0xF1:Customer Option Others: Reserved
8 ~ 0	IAPSNB[8:0]	IAP operation sector number setting during sector/page erase: Starting address of the actual operating sector = Flash base address + [IAPSNB[8:0] x 0x200]
23 ~ 9	-	Reserved

5.14.1.3 IAP control register IAP_CON (write protection)

***This register is write-protected and can only be modified by operating the Data Protection Register IAP_KEY.**

Register	Read/Write	Description	Reset Value
IAP_CON	R/W	IAP Control Register	0x0000_0000

31	30	29	28	27	26	25	24
LOCK	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	BTLD[1:0]		RST
7	6	5	4	3	2	1	0
ERASE	-	SERASE	PRG	-	-	CMD[1:0]	

Bit Number	Bit Symbol	Description
31	LOCK	After writing 1 to this bit, the IAP_CON Register is locked. When the unlock sequence is detected, hardware clears this bit to 0. If the unlock operation fails, this bit remains set to 1 until the next System Reset.
10 ~ 9	BTLD[1:0]	Application Start Area Selection Bit after Software Reset: 00: Chip boots from APROM (Application Program ROM) after Software Reset 01: Chip boots from LDROM (system storage area) after Software Reset 10: Chip boots from Embedded SRAM after Software Reset 11: Reserved
8	RST	Software Reset Control Bit 0: Normal Program Operation 1: Writing 1 to this bit triggers an immediate system reset
7	ERASE	Chip Erase / Full Erase Control Bit 0: No Operation 1: Writing 1 to this bit and then setting CMD[1:0] = 10 initiates APROM Chip Erase / Full Erase, erasing the entire APROM
5	SERASE	Sector Erase Control Bit 0: No Operation 1: Writing 1 to this bit and then setting CMD[1:0] = 10 initiates APROM Sector Erase, erasing the specified APROM Sector
4	PRG	Programming Control Bit 0: Disable Flash Programming 1: Enable Flash Programming
1 ~ 0	CMD[1:0]	IAP Command Enable Control Bit 10: Execute Erase Operation Command Others: Reserved Note:

Bit Number	Bit Symbol	Description
		- After setting the Erase operation command bit to 1, CMD[1:0] must be configured to 10 for the operation to start - Only one IAP operation can be executed at a time, so only one of the ERASE or SERASE bits can be set to 1 simultaneously
30 ~ 11 6 3 ~ 2	-	Reserved

5.14.1.4 IAP register mapping

Register	Offset Address	Read/Write	Description	Reset Value
IAP base address: 0x4000_03C0				
IAP_KEY	0x00	R/W	Data Protection Register	0x0000_0000
IAP_SNB	0x04	R/W	IAP Sector Number Setting Register	0x0000_0000
IAP_CON	0x0C	R/W	IAP Control Register	0x0000_0000

5.15 Option byte area (Customer Option)

The SC32F11T/11G features a dedicated Flash area for storing customers' power-on initial settings, called the Customer Option area. During programming, users can configure Customer Option items via the Host Software. The configuration values are written into the Customer Option area, and the IC uses this Customer Option data as initial settings during reset initialization.

Customer Option items can also be temporarily modified by manipulating the Customer Option mapping register. However, **please note that changes to the mapping register only provide temporary adjustments** and do not alter the values stored in the Customer Option area. After a chip reset, initialization will always follow the Customer Option parameters set during programming.

The operation method of Customer Option related Mapping Registers is as follows:

The read and write operations of Customer Option related SFRs are controlled by two registers, OPINX and OPREG. The specific location of each Customer Option SFR is determined by OPINX, as shown in the table below:

Register	Address	Description	Reset Value
OPINX	0x4000_03F8	Customer Option Pointer	0x0000_0000
OPREG	0x4000_03FC	Customer Option Register	0x0000_0000
OPT_CON0	0XC1 @ OPINX	Customer Option Mapping Register 0	0x0000_0000
OPT_CON1	0XC2 @ OPINX	Customer Option Mapping Register 1	0x0000_0000

5.15.1 Mapping register for Customer Option

Before rewriting the IFB mapping register using OPINX with OPREG, ensure the clock enable switch AHB_CFG.IFBEN for the Customer Option Register is first turned on:

5.15.1.1 Ahb bus peripheral clock enable register (AHB_CFG)

Register	Read/Write	Description	Reset Value
AHB_CFG	R/W	AHB Bus Peripheral Clock Enable Register	0x0020_0000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	CLKDIV[2:0]			-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	CANEN	-	IFBEN	CRCEN	DMAEN

Bit Number	Bit Symbol	Description
2	IFBEN	Customer Option Mapping Register Clock Enable Bit Before rewriting the IFB Mapping Register using OPINX with OPREG, the Clock Enable must be enabled first. 0: Disable 1: Enable
31 ~ 23 19 ~ 5 3	-	Reserved

5.15.1.2 Customer Option mapping register 0 OPT_CON0

Register	Read/Write	Description	Reset Value
OPT_CON0	R/W	Customer Option Mapping Register 0	0x0000_0000

7	6	5	4	3	2	1	0
-	-	-	-	-	DISLVR	LVRS[1:0]	

Bit Number	Bit Symbol	Description
2	DISLVR	LVR Switch 0: LVR Enabled 1: LVR Disabled
1 ~ 0	LVRS[1:0]	LVR Voltage Selection Control 11: 4.3 V Reset 10: 3.7 V Reset 01: 2.9 V Reset 00: 1.9 V Reset
7 ~ 3	-	Reserved

5.15.1.3 Customer Option mapping register 1 OPT_CON1

Register	Read/Write	Description	Reset Value
OPT_CON1	R/W	Customer Option Mapping Register 1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	HIRC_PLL	DRV_EH	-	OP_BL[1:0]	

Bit Number	Bit Symbol	Description
7	ENWDT	WDT Switch 1: WDT Enabled 0: WDT Disabled

Bit Number	Bit Symbol	Description
6	DISJTG	JTAG Port Switching Control Bit 0: JTAG Mode Enable, corresponding pins can only be used as T_CLK/ T_DIO 1: Normal Mode, JTAG function disabled
5	DISRST	Reset Signal Port Switch Control Bit This bit is read-only and cannot be modified by the user. 0: The RST pin is used as a reset pin. 1: The RST pin is used as a normal GPIO pin.
4	HIRC_PLL	PLL Clock Source Switch Control Bit 0: PLL 1: Select HIRC/1 to replace PLL (when used, set RCC_CFG0.HIRC_NDIV to 1)
3	DRV_EH	IOL Drive Capability Selection for the Port with COM: 0: For ports corresponding to COM0 through COM7, IOL has strong drive capability only when the port is enabled for COM function; otherwise, the port maintains normal drive capability. For applications without COM driving, it is recommended to use the normal drive capability for these ports. 1: Ports COM0 to COM7 have a Drive Capability with the sinking current IOL always strong.
1 ~ 0	OP_BL[1:0]	Boot area selection after chip Reset This bit is read-only and cannot be modified by the user. 00: Boot from APROM (Application Program ROM) after chip Reset 01: Boot from LDROM (system storage area) after chip Reset 10: Boot from Embedded SRAM after chip Reset 11: Reserved
2	-	Reserved

6 Power, reset and system clock (RCC)

6.1 Power-on process

After power-on of the SC32F11T/11G, the client software execution will proceed through the following three stages:

1. Reset Stage
2. Loading Information Stage
3. Normal Operation Stage.

6.1.1 Reset stage

The Reset Stage refers to the SC32F11T/11G being continuously held in the reset state until the power supply voltage exceeds a specific threshold, at which point its internal clock mechanism begins to operate effectively.

The exact duration of this stage depends on the rise rate of the external power supply voltage. When the external power supply voltage reaches the built-in POR voltage, the Reset Stage ends.

6.1.2 Loading information stage

An internal warm-up counter is provided inside the SC32F11T/11G. During the reset stage, this warm-up counter is kept at zero. After the supply voltage rises to POR, the internal HIRC oscillator warm-up counter starts counting. When the warm-up counter reaches a certain value, the IFB data (including Customer Option) in Flash ROM will be periodically read to the system register. After all IFB data is read, the warm-up and information loading stages end, and the system enters normal operating mode.

6.1.3 Normal operation stage

After the Loading Information Stage ends, the SC32F11T/11G begins fetching instruction codes from Flash and enters the Normal Operation Stage. At this point, the LVR voltage is the setting value configured by the user in the Customer Option.

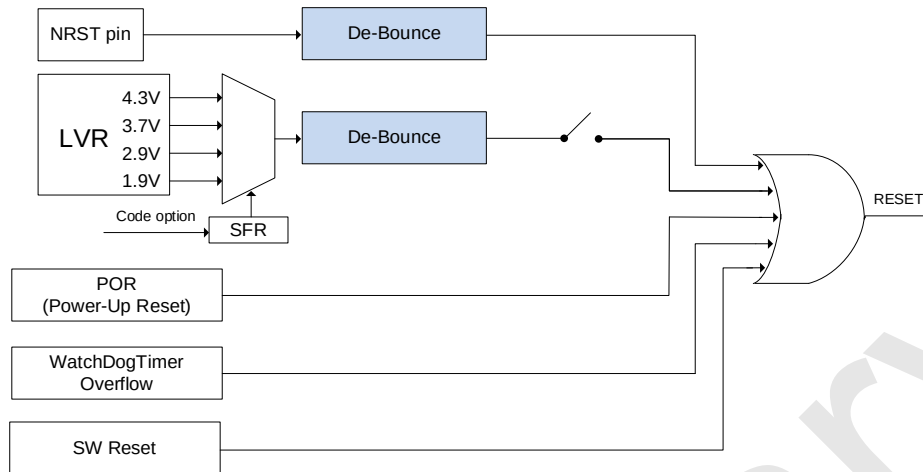
6.2 Reset

The SC32F11T/11G supports two types of Reset: Hardware Reset and Software Reset. When a Reset occurs, all registers except for the CAN registers will be restored to their Reset Value. For the Reset Value of the CAN registers, please refer to the CAN registers section in the SC32F11T/11G_TRM.

The SC32F11T/11G has five Reset types, the first four of which are Hardware Reset:

1. External RST Reset
2. Low Voltage Reset (LVR)
3. Power-On Reset (POR)
4. Watchdog (WDT) Reset
5. Software Reset

The circuit diagram of the reset section of the SC32F11T/11G is shown below:



SC32F11T/11G Reset Circuit Diagram

6.2.1 Hardware reset

Hardware Reset can be performed by the following four methods:

1. External RST Reset
2. Low Voltage Reset (LVR)
3. Power-On Reset (POR)
4. Watchdog (WDT) Reset

6.2.1.1 External RST reset

The external RST Reset of SC32F11T/11G is triggered by applying a low-level reset pulse longer than 18 μ s to the external NRST pin.

Before programming, users can configure the PD3 / NRST pin as NRST (Reset pin) via the Customer Option in the Host Software.

- When this pin is configured as a reset function, it cannot serve as GPIO.
- When this pin is configured as GPIO, its reset function is disabled.

6.2.1.2 Low voltage reset (LVR)

SC32F11T/11G includes a built-in Low Voltage Reset circuit. There are four options for the reset threshold voltage: 4.3 V, 3.7 V, 2.9 V, and 1.9 V. The factory default is set to 1.9 V, but users can adjust the default by configuring the Customer Option value during flashing. When the V_{DD} Voltage drops below the set threshold and remains there for longer than the debounce time T_{LVR} of about 30 μ s, the chip will be Reset.

6.2.1.3 Power-on reset (POR)

The SC32F11T/11G contains an internal Power-On Reset circuit; the system automatically Resets when the power supply voltage V_{DD} reaches the POR reset voltage.

6.2.1.4 Watchdog reset WDT

The SC32F11T/11G features a WDT with its Clock Source as the internal 37 kHz Oscillator. Users can

enable or disable the Watchdog Reset function via the programmer's Customer Option. A Watchdog Reset will occur if a watchdog event takes place.

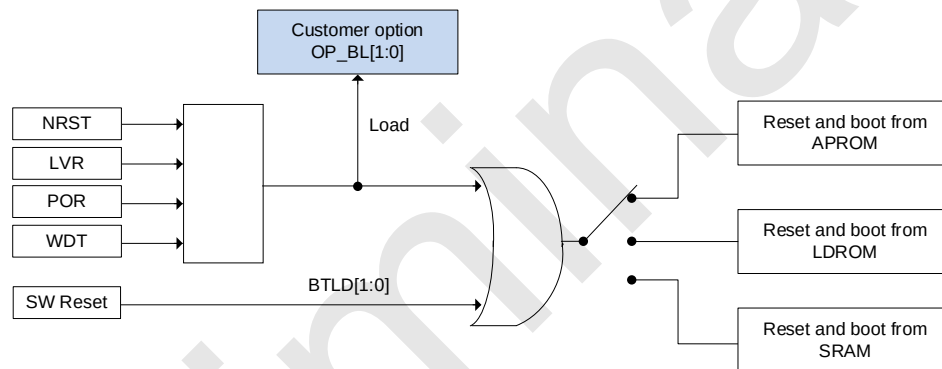
6.2.2 Software reset

The SC32F11T/11G provides a Software Reset feature. Users can set RST (IAP_CON.8) to 1 to immediately carry out a Software Reset of the system.

6.2.3 Boot area after reset

After the four hardware reset types-External RST Reset, Low Voltage Reset (LVR), Power-On Reset (POR), and Watchdog (WDT)-the chip boots from the boot area (APROM / LDROM / SRAM) specified by the user OP_BL[1:0].

After a software reset, the chip boots from the boot area (APROM / LDROM / SRAM) specified by BTLD[1:0].



SC32F11T/11G Reset Boot Area Switching Diagram

6.2.4 Initial reset state

When the SC32F11T/11G is in reset state, most registers return to their initial values. The Watchdog WDT function is disabled during this period. Resets during 'Hot-start' (such as WDT, LVR, software reset, etc.) do not affect SRAM data; thus, SRAM retains the pre-reset values.

Note: If the power supply voltage falls below the level required to maintain RAM data retention, the contents of SRAM will be lost.

6.3 Clock

6.3.1 System clock source

System Clock SYSCLK can be driven by five different clock sources:

- Built-in high-frequency 64 MHz Oscillator (HIRC)
- External high-frequency Crystal, supporting external connection to a 2 to 16 MHz high-frequency oscillator (HXT)
- Built-in low-frequency 37 kHz Oscillator (LIRC)
- External low-frequency Crystal Oscillator, can connect to a 32.768 kHz low-frequency oscillator (LXT)

- PLL, with a maximum frequency of 72 MHz.

Each oscillator can be individually enabled or disabled to reduce power consumption when not in use.

Note:

1. **The default system clock source at power-up is HIRC, and the default system clock frequency is $f_{HIRC}/2$. Users can switch the clock source by software during the Normal Operation Stage after power-up. Before switching, ensure the selected clock source is in a stable operating state**
2. **When switching the System Clock Source, you must first switch to HIRC before switching to the target Clock Source.**

6.3.2 Built-in high-frequency 64 MHz oscillator (HIRC)

The built-in high-frequency clock HIRC can be enabled by setting the HIRCEN bit of Register RCC_CFG0 to 1, or disabled by clearing it to 0. The user must first write a value exceeding 0x40 to RCC Protection Register RCC_KEY before modifying RCC_CFG0 and RCC_CFG1.

HIRC has the following Features:

- Can serve as the System Operating Clock.
- The default clock frequency when power on f_{SYS} is $f_{HIRC}/2$.
- Frequency error: $\leq \pm 1\%$ across the operating conditions of 2.0 V to 5.5 V and -40 to 105 °C;
- The system clock can be automatically calibrated by the 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to that of the external 32.768 kHz crystal oscillator.

6.3.3 Built-in high-frequency crystal oscillator circuit, can be externally connected to a 2 to 16 MHz high-frequency oscillator (HXT)

The external high-frequency crystal oscillator clock (HXT) can be enabled by setting the HXTEN bit of Register RCC_CFG0 to 1, or disabled by clearing it to 0; The user must first write a value exceeding 0x40 to RCC Protection Register RCC_KEY before modifying RCC_CFG0 and RCC_CFG1.

Additionally, users must set an appropriate CRY_HF value according to the frequency of the externally connected high-frequency crystal oscillator. When the frequency is below 12 MHz, CRY_HF should be set to 0; When the frequency is above 12 MHz, CRY_HF should be set to 1.

HXT provides the following functions and features:

- Can serve as the System Operating Clock.
- Supports external connection of a 2 to 16 MHz high-frequency oscillator.

6.3.4 Built-in low-frequency 37 kHz oscillator (LIRC) .

The built-in low-frequency clock LIRC can be enabled by setting LIRCEN to 1 in Register RCC_CFG0, or disabled by clearing it to 0; The user must first write a value exceeding 0x40 to RCC Protection Register RCC_KEY before modifying RCC_CFG0 and RCC_CFG1.

LIRC has the following functions and features:

- Can serve as the System Operating Clock.
- Can serve as the clock source for LCD/LED modules
- Can serve as the clock source for the Base Timer and WDT; when WDT is enabled, this clock source must be enabled

- Frequency error: Within the voltage range of 2.0 to 5.5 V and at normal temperature of 25 °C, the frequency error after register correction is $\leq \pm 4\%$.

6.3.5 Built-in low frequency oscillator circuit, with support for external 32.768 kHz low frequency oscillator (LXT)

When using an external low-frequency Crystal clock LXT, enable it by setting the LXTEN bit of Register RCC_CFG0 to 1, or disable it by clearing to 0; The user must first write a value exceeding 0x40 to RCC Protection Register RCC_KEY before modifying RCC_CFG0 and RCC_CFG1.

LXT has the following functions and features:

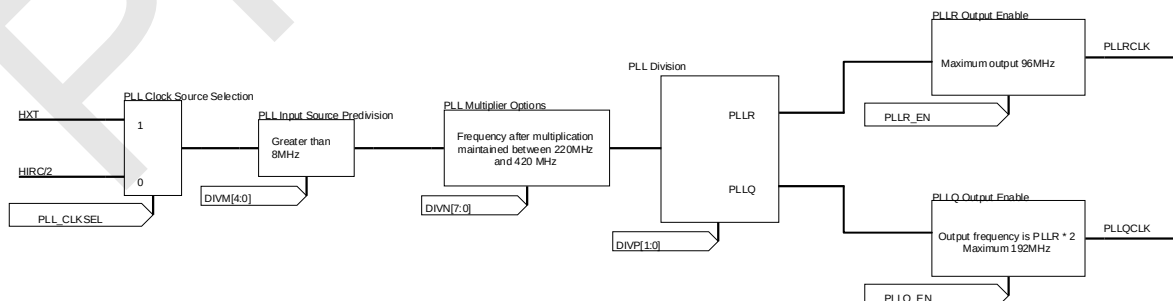
- Can serve as the System Operating Clock.
- Can be selected as the Base Timer clock source
- Can serve as the clock source for LCD/LED modules
- Supports an external 32.768 kHz low-frequency oscillator.
- Automatic calibration of HIRC can be performed using LXT.

6.3.6 PLL

PLL, output can be divided into PLLRCLK and PLLQCLK.

PLL has the following functions and features:

- PLLRCLK
 - Can be selected as Application Output, with output frequency up to 96 MHz.
 - Can be selected as the System Clock Source, with output frequency up to 72 MHz.
- PLLQCLK
 - Output frequency is twice that of PLLRCLK, up to 192 MHz.
 - Can be selected as the PWM0 clock source.
- Users can configure the required frequency using the following formula:
 - PLL input clock frequency f_{PLL_IN}
 - PLL output frequency $f_{PLL} = [(f_{PLL_IN} / DIVM) * (DIVN+2)] / 2 ^ (DIVP +1)$
- The block diagram of the PLL circuit is as follows:



6.4 Register access clock and peripheral clock source

6.4.1 Register access clock

The register access clock drives the Cortex®-M0+ core and internal bus operations. This clock directly drives the instruction execution pipeline, register group access, and data transfer between the core and the bus.

The register access clock remains strictly synchronous with the AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) bus clocks, ensuring coordinated operation of the CPU core and peripheral interfaces within a unified timing framework. Users must enable bus clocks and control peripheral clock gating via the AHB Bus Peripheral Clock Enable Register (AHB_CFG) or the APB Bus Peripheral Clock Enable Registers (APBn_CFG, n=0 to 2). Read and write operations to a peripheral register can only be performed when both the bus and the register access clock bits for the corresponding peripheral are enabled; otherwise, a hardware protection mechanism will be triggered, invalidating the access.

6.4.2 Peripheral clock source

The Peripheral Clock Source is a clock signal source that provides independent operating clock ticks for specific peripheral modules (such as PWM, UART, ADC, etc.). It can be a divided or multiplied version of the System Clock, or an independent built-in or external Clock Source (such as an internal RC Oscillator or an external Crystal Oscillator). The Peripheral Clock Source allows different peripherals to select the optimal Clock Frequency and stability based on their own needs. Users can also reduce Power Consumption by disabling clocks for unused peripherals individually.

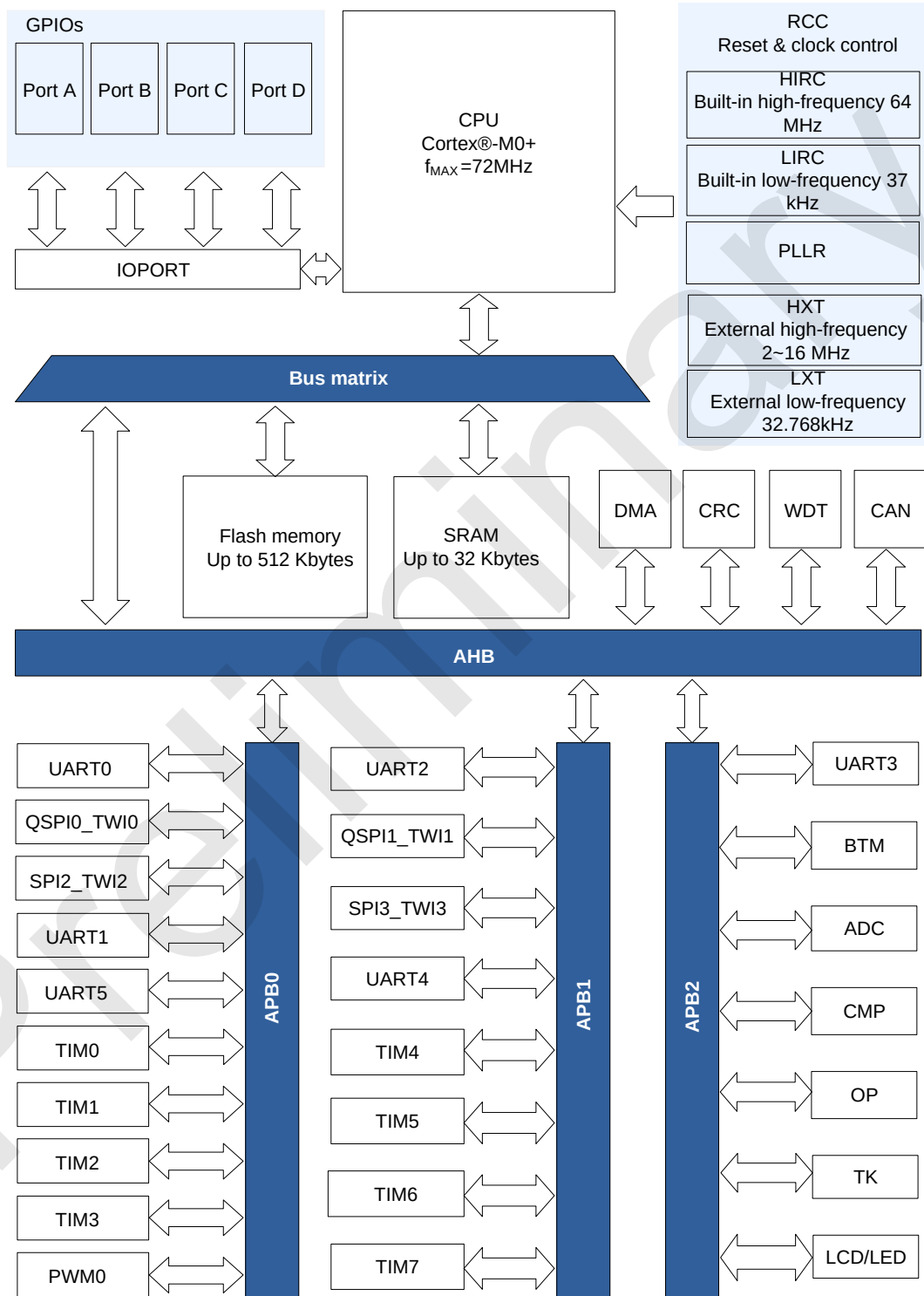
Some peripherals of the SC32F11T/11G provide multiple optional Clock Sources. Users can select the appropriate Clock Source for peripherals through the Peripheral Clock Source selection registers (RCC_CFGn, n=0 to 1).

6.4.3 Bus clock

Users may configure the frequencies of the IOPORT, AHB, APB0, APB1, and APB2 domains using multiple prescalers.

- IOPORT: The main clock for the GPIO port domain, derived by dividing the System Clock SYSCLK, with a maximum frequency of 72 MHz. All GPIOs are driven by IOPORT.
- HCLK: The main clock for the AHB domain, derived by dividing the System Clock SYSCLK. It defaults to half the system clock frequency and can be adjusted via the CLKDIV[2:0] bits in the AHB CFG register. The maximum frequency is 72 MHz. HCLK drives peripherals including the Cortex®-M0+ Core, Memory, and DMA.
- PCLK0: The main clock for the APB0 domain, derived by dividing HCLK, with a maximum frequency equal to HCLK. All peripherals on the APB0 Bus are driven by PCLK0, and some peripheral clock sources on the Bus are provided by PCLK0.
- PCLK1: The main clock for the APB1 domain, derived by dividing HCLK. Its maximum frequency equals that of HCLK. All peripherals on the APB1 bus are driven by PCLK1, and some peripheral clock sources on the bus come from PCLK1.
- PCLK2: The main clock for the APB2 domain, derived by dividing HCLK. Its maximum frequency equals that of HCLK. All peripherals on the APB2 bus are driven by PCLK2, and some peripheral clock sources on the bus come from PCLK2.

The bus architecture diagram is shown below. The frequency for reading peripheral registers depends on the frequency of the bus to which the peripheral is connected.



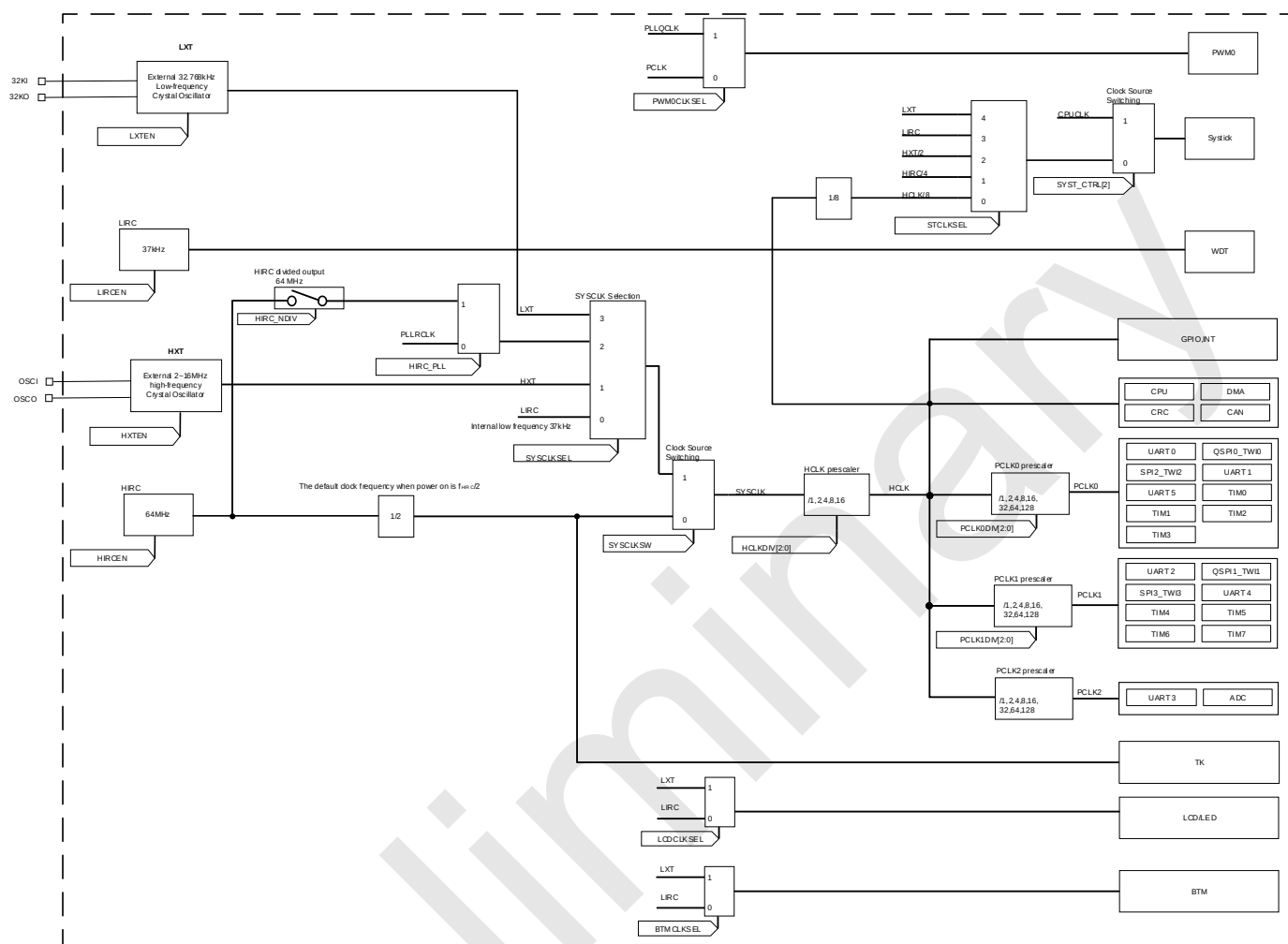
Bus Architecture Block Diagram

6.4.4 Peripheral clock

Peripheral Clocks on the Bus are generally provided by their corresponding Bus Clocks, but the following peripherals can select other Clock Sources:

- PWM0 can select the following Clock Sources:
 - PCLK, the Clock on the Bus that PWM0 resides on
 - PLLQCLK
- LCD/LED can select the following Clock Sources:
 - LIRC, the internal low-frequency Clock
 - LXT, the Low-frequency Crystal Clock
- BTM can select the following Clock Sources:
 - LIRC, the internal low-frequency Clock
 - LXT, the Low-frequency Crystal Clock
- The WDT Clock Source is fixed to LIRC; when WDT is enabled, LIRC automatically starts, and it remains oscillating during WDT operation, which cannot be turned off by the user.
- SysTick can select the following Clock Sources:
 - LXT, the Low-frequency Crystal Clock
 - LIRC, the internal low-frequency Clock
 - HXT/2, the High-frequency Crystal Clock divided by 2
 - HIRC/4, the clock divided from the internal high-frequency clock by 4
 - HCLK/8, the clock divided from the AHB Bus clock by 8
 - CPUCLK, the Core clock

6.4.5 Peripheral clock block diagram



Note: The default clock frequency when powered on, f_{SYS} , is $f_{\text{HIRC}}/2$; users can select the desired clock source by modifying `SYSCLKSW` or `SYSCLKSEL` bits.

6.4.6 Peripheral clock enable register

Each peripheral clock can be enabled via the corresponding enable bits in the AHB_CFG and APBn_CFG registers. When the peripheral clock is inactive, read and write access to the peripheral registers is disabled.

6.4.7 Low-power mode clock

In low power STOP mode, the CPU clock, most clock sources, and peripheral clocks stop, and the program halts execution. However, the following clock sources continue to operate normally in low power STOP mode:

- Internal low frequency clock LIRC
- External low frequency oscillator clock LXT

6.5 RCC interrupt

Supporting the oscillation stop detection mechanism, the clock source of SC32F11T/11G provides a user-configurable RCC Interrupt: when the system clock source is HXT, if an abnormality in the clock source is

detected, the oscillation stop detection interrupt flag is set. If the corresponding interrupt is enabled, an oscillation stop detection interrupt is triggered.

Preliminary

7 Interrupts

- The M0+ core supports up to 32 interrupt sources, numbered 0 to 31; the SC32F11T/11G Series includes 25 interrupt sources in total.
- Four interrupt priority levels are configurable. Interrupt priorities are set via the core's Interrupt priority registers.

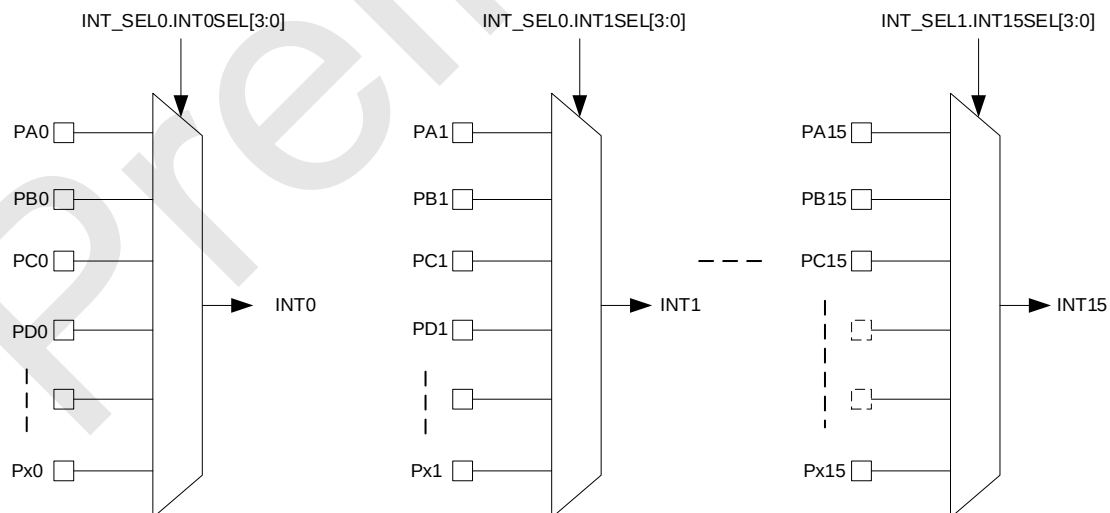
7.1 External interrupts INT0 to INT15

There are 16 external interrupt sources that share 4 interrupt vectors. All 16 sources can be configured to trigger on Rising Edge, Falling Edge, or Both Edge. Once configured, they can map to any GPIO pin. Setting the corresponding interrupt flag (RIF/FIF = 1) in software triggers the respective interrupt.

The external interrupt features of the SC32F11T/11G Series are as follows:

- There are 16 INT interrupt sources, collectively occupying 4 interrupt vectors.
- After switching INT settings, they can be assigned to all GPIO pins.
- All can be configured for Rising Edge, Falling Edge, or Both Edge interrupts, each with an independent corresponding Interrupt Flag.
- Setting the corresponding Interrupt Flag via software can trigger the corresponding interrupt.

Note: When switching INT functions, users must manually set the GPIO Port of INT_n (n=0 to 15) to input mode with Pull-up enabled; external interrupts cannot be detected when the port is in output mode.



7.2 Interrupt and events

- When NVIC is disabled, the interrupt request mask bit is enabled, generating events without generating Interrupts.
- After NVIC is enabled, the interrupt request mask bit serves as the module's global Interrupt switch.

7.3 Interrupt vector table

Interrupts Vector number	Interrupts	Priority	Interrupt Vector Address	Interrupt sources	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Sub Switch	Interrupt Flag Bit	Wake up from stop
0	-	-	0x0000_0000	-		-	\	\	YES
1	-	Fixed	0x0000_0004	RESET	PRIMASK	SCB	\	\	YES
2	-	Fixed	0x0000_0008	NMI_Handler		SCB	\	\	YES
3	-	Fixed	0x0000_000C	HardFault_Handler	PRIMASK	SCB	\	\	YES
4 ~ 10	-	-	0x0000_0010 - 0x0000_0028	-		-	\	\	YES
11	-	Configurable		SVC_Handler	PRIMASK	SCB	\	\	YES
12 ~ 13	-	-	0x0000_0030 0x0000_0034	-		-	\	\	YES
14	-	Configurable	0x0000_0038	PendSV_Handler	PRIMASK	SCB	\	\	YES
15	-	Configurable	0x0000_003C	SysTick_Handler	PRIMASK	SysTick_CTRL	\	\	NO
16	0	Configurable	0x0000_0040	INT0	NVIC->ISER[0].0	INTF_IE->ENF _x ,x=0 INTR_IE->ENR _x	\	INTF_STS->FIF _x INTR_STS->RIF _x	YES
17	1	Configurable	0x0000_0044	INT1-7	NVIC->ISER[0].1	INTF_IE->ENF _x ,x=1 to 7 INTR_IE->ENR _x	\	INTF_STS->FIF _x INTR_STS->RIF _x	YES
18	2	Configurable	0x0000_0048	INT8-11	NVIC->ISER[0].2	INTF_IE->ENF _x ,x=8 to 11 INTR_IE->ENR _x	\	INTF_STS->FIF _x INTR_STS->RIF _x	YES
19	3	Configurable	0x0000_004C	INT12-15	NVIC->ISER[0].3	INTF_IE->ENF _x ,x=12 to 15 INTR_IE->ENR _x	\	INTF_STS->FIF _x INTR_STS->RIF _x	YES
20	4	Configurable	0x0000_0050	RCC Stop Oscillation Detection	NVIC->ISER[0].4	RCC_CFG->INTEN	\	RCC_STS->CLKFIF	NO
21	5	Reserved	0x0000_0054	\	NVIC->ISER[0].5	\	\	\	
22	6	Configurable	0x0000_0058	BTM	NVIC->ISER[0].6	BTM_CON->INTEN	\	BTM_STS->BTMIF	YES
23	7	Configurable	0x0000_005C	UART0	NVIC->ISER[0].7	UART0_IDE->INTEN	UART0_IDE->TXIE UART0_IDE->RXIE	UART0_STS->TXIF UART0_STS->RXIF	YES
				UART2	\	UART2_IDE->INTEN	UART2_IDE->TXIE UART2_IDE->RXIE	UART2_STS->TXIF UART2_STS->RXIF	YES

Interrupts Vector number	Interrupts	Priority	Interrupt Vector Address	Interrupt sources	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Sub Switch	Interrupt Flag Bit	Wake up from stop
				UART4	\	UART4_IDE->INTEN	UART4_IDE->TXIE UART4_IDE->RXIE	UART4_STS->TXIF UART4_STS->RXIF	YES
24	8	Configurable	0x0000_0060	UART1	NVIC->ISER[0].8	UART1_IDE->INTEN	UART1_IDE->TXIE UART1_IDE->RXIE	UART1_STS->TXIF UART1_STS->RXIF	YES
				UART3	\	UART3_IDE->INTEN	UART3_IDE->TXIE UART3_IDE->RXIE	UART3_STS->TXIF UART3_STS->RXIF	YES
				UART5	\	UART5_IDE->INTEN	UART5_IDE->TXIE UART5_IDE->RXIE	UART5_STS->TXIF UART5_STS->RXIF	YES
				QSPI0/SPI0/TWI0	NVIC->ISER[0].9	TWI_QSPI0_IDE->INTEN	TWI_QSPI0_IDE->QTWIE TWI_QSPI0_IDE->RXNEIE TWI_QSPI0_IDE->TBIE TWI_QSPI0_IDE->RXIE TWI_QSPI0_IDE->RXHIE TWI_QSPI0_IDE->TXHIE	TWI_QSPI0_STS->QTWIF TWI_QSPI0_STS->RXNEIF TWI_QSPI0_STS->TXEIF TWI_QSPI0_STS->RXFIF TWI_QSPI0_STS->RXHIF TWI_QSPI0_STS->TXHIF	NO
25	9	Configurable	0x0000_0064	SPI2/TWI2		TWI_SPI2_IDE->INTEN	TWI_QSPI2_IDE->TBIE	TWI_QSPI2_STS->QTWIF TWI_QSPI2_STS->TXEIF	NO
26	10	Configurable	0x0000_0068	QSPI1/SPI1/TWI1	NVIC->ISER[0].10	TWI_QSPI1_IDE->INTEN	TWI_QSPI1_IDE->QTWIE TWI_QSPI1_IDE->RXNEIE TWI_QSPI1_IDE->TBIE TWI_QSPI1_IDE->RXIE TWI_QSPI1_IDE->RXHIE TWI_QSPI1_IDE->TXHIE	TWI_QSPI1_STS->QTWIF TWI_QSPI1_STS->RXNEIF TWI_QSPI1_STS->TXEIF TWI_QSPI1_STS->RXFIF TWI_QSPI1_STS->RXHIF TWI_QSPI1_STS->TXHIF	NO
				SPI3/TWI3		TWI_SPI3_IDE->INTEN	TWI_QSPI3_IDE->TBIE	TWI_QSPI3_STS->QTWIF TWI_QSPI3_STS->TXEIF	NO
27	11	Configurable	0x0000_006C	DMA0	NVIC->ISER[0].11	DMAAn_CFG->INTEN	DMAAn_CFG->TCIE DMAAn_CFG->HTIE DMAAn_CFG->TEIE	DMAAn_STS->GIF DMAAn_STS->TCIF DMAAn_STS->HTIF DMAAn_STS->TEIF	NO
28	12	Configurable	0x0000_0070	DMA1	NVIC->ISER[0].12	DMAAn_CFG->INTEN	DMAAn_CFG->TCIE DMAAn_CFG->HTIE DMAAn_CFG->TEIE	DMAAn_STS->GIF DMAAn_STS->TCIF DMAAn_STS->HTIF DMAAn_STS->TEIF	NO
29	13	Configurable	0x0000_0074	DMA2	NVIC->ISER[0].13	DMAAn_CFG->INTEN	DMAAn_CFG->TCIE DMAAn_CFG->HTIE DMAAn_CFG->TEIE	DMAAn_STS->GIF DMAAn_STS->TCIF DMAAn_STS->HTIF DMAAn_STS->TEIF	NO
30	14	Configurable	0x0000_0078	DMA3	NVIC->ISER[0].14	DMAAn_CFG->INTEN	DMAAn_CFG->TCIE DMAAn_CFG->HTIE DMAAn_CFG->TEIE	DMAAn_STS->GIF DMAAn_STS->TCIF DMAAn_STS->HTIF DMAAn_STS->TEIF	NO
31	15	Configurable	0x0000_007C	TIM0	NVIC->ISER[0].15	TIM0_IDE->INTEN	TIM0_IDE->TIE TIM0_IDE->EXFIE TIM0_IDE->EXRIE	TIM0_STS->TIF TIM0_STS->EXFIF TIM0_STS->EXIR	NO

Interrupts Vector number	Interrupts	Priority	Interrupt Vector Address	Interrupt sources	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Sub Switch	Interrupt Flag Bit	Wake up from stop
32	16	Configurable	0x0000_0080	TIM1	NVIC->ISER[0].16	TIM1_IDE->INTEN	TIM1_IDE->TIE TIM1_IDE->EXFIE TIM1_IDE->EXRIE	TIM1_STS->TIF TIM1_STS->EXIF TIM1_STS->EXIR	NO
33	17	Configurable	0x0000_0084	TIM2	NVIC->ISER[0].17	TIM2_IDE->INTEN	TIM2_IDE->TIE TIM2_IDE->EXFIE TIM2_IDE->EXRIE	TIM2_STSSR->TIF TIM2_STS->EXIF TIM2_STS->EXIR	NO
34	18	Configurable	0x0000_0088	TIM3	NVIC->ISER[0].18	TIM3_IDE->INTEN	TIM3_IDE->TIE TIM3_IDE->EXFIE TIM3_IDE->EXRIE	TIM3_STS->TIF TIM3_STS->EXIF TIM3_STS->EXIR	NO
35	19	Configurable	0x0000_008C	TIM4	NVIC->ISER[0].19	TIM4_IDE->INTEN	TIM4_IDE->TIE TIM4_IDE->EXFIE TIM4_IDE->EXRIE	TIM4_STS->TIF TIM4_STS->EXIF TIM4_STS->EXIR	NO
				TIM5	\	TIM5_IDE->INTEN	TIM5_IDE->TIE TIM5_IDE->EXFIE TIM5_IDE->EXRIE	TIM5_STS->TIF TIM5_STS->EXIF TIM5_STS->EXIR	NO
36	20	Configurable	0x0000_0090	TIM6	NVIC->ISER[0].20	TIM6_IDE->INTEN	TIM6_IDE->TIE TIM6_IDE->EXFIE TIM6_IDE->EXRIE	TIM6_STS->TIF TIM6_STS->EXIF TIM6_STS->EXIR	NO
				TIM7	\	TIM7_IDE->INTEN	TIM7_IDE->TIE TIM7_IDE->EXFIE TIM7_IDE->EXRIE	TIM7_STS->TIF TIM7_STS->EXIF TIM7_STS->EXIR	NO
37	21	Configurable	0x0000_0094	PWM0	NVIC->ISER[0].21	PWM0_CON->INTEN	\	PWM0_STS->PWMIF	NO
38	22	Reserved	0x0000_0098	\	NVIC->ISER[0].22	\	\	\	
39	23	Reserved	0x0000_009C	\	NVIC->ISER[0].23	\	\	\	
40	24	Reserved	0x0000_00A0	\	NVIC->ISER[0].24	\	\	\	
41	25	Reserved	0x0000_00A4	\	NVIC->ISER[0].25	\	\	\	
42	26	Reserved	0x0000_00A8	\	NVIC->ISER[0].26	\	\	\	
43	27	Reserved	0x0000_00AC	\	NVIC->ISER[0].27	\	\	\	
44	28	Configurable	0x0000_00B0	CAN	NVIC->ISER[0].28	\	CAN_RTIE->RIE CAN_RTIE->ROIE CAN_RTIE->RFIE CAN_RTIE->RAFIE CAN_RTIE->TPIE CAN_RTIE->TSIE CAN_RTIE->EIE CAN_RTIE->EPIE	CAN_RTIE->RIF CAN_RTIE->ROIF CAN_RTIE->RFIF CAN_RTIE->RAFIF CAN_RTIE->TPIF CAN_RTIE->TSIF CAN_RTIE->EIF CAN_RTIE->EPIF	NO

Interrupts Vector number	Interrupts	Priority	Interrupt Vector Address	Interrupt sources	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Sub Switch	Interrupt Flag Bit	Wake up from stop
							CAN_RTIE->ALIE CAN_RTIE->BEIE	CAN_RTIE->ALIF CAN_RTIE->BEIF	
45	29	Configurable	0x0000_00B4	ADC	NVIC->ISER[0].29	ADC_CON->INTEN	\	ADC_STS->ADCIF	NO
46	30	Configurable	0x0000_00B8	CMP	NVIC->ISER[0].30	CMPCFG->CMPIM[1:0]	\	CMP_STS->CMPIF	YES
47	31	Configurable	0x0000_00BC	TK	NVIC->ISER[0].31	TKCON->INTEN	\	TKCON->TKIF	YES

8 Power saving mode

After initial power-up, the system runs by default in Normal Mode, with three additional power saving modes available:

- Low-Speed Mode: The system clock source can be selected as LIRC, allowing the CPU to operate at 37 kHz.
- IDLE Mode, which can be woken by any interrupt.
- STOP Mode, which can be woken by INT0 to 15, Base Timer, UART, TK, and CMP.

9 GPIO

9.1 Clock source

The M0+ core can access GPIO through the IOPORT bus in a single cycle, resulting in extremely high data transfer efficiency. The clock for the IOPORT bus is derived from HCLK.

9.2 Feature

The GPIO Port Features of the SC32F11T/11G Series are as follows:

- Up to 60 bidirectional GPIOs independently controllable
- The CPU can access GPIO ports via the IOPORT bus within a single cycle
- Independent pull-up resistor configuration is available
- Drive Capability of the COM port can reach 100 mA@0.8 V
- Drive Capability of the conventional port can reach 55 mA@0.8 V
- 16 GPIOs per group
- In both input and output states, the actual status value of the port can be read from the port data register.

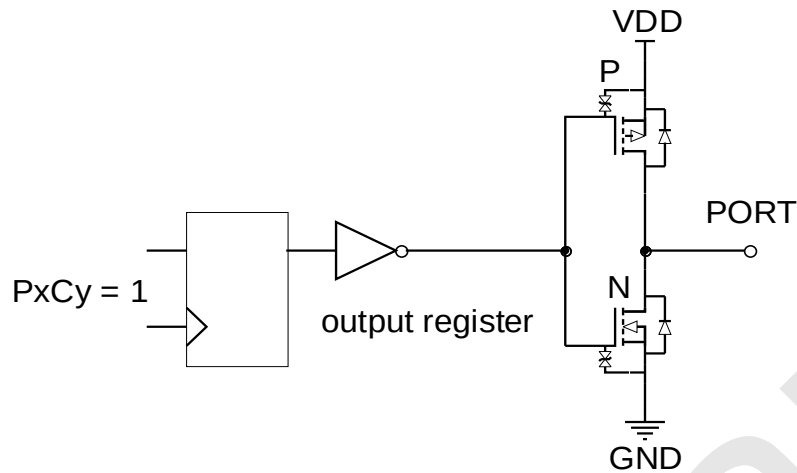
Note: Unused ports and ports not exposed in the package must be set to strong push-pull output mode.

9.3 GPIO block diagram

9.3.1 Strong push-pull output mode

In strong push-pull output mode, continuous high-current drive is available: see the [《GPIO Parameter》](#) section for detailed electrical specifications.

The port structure schematic diagram under strong push-pull output mode is as follows:

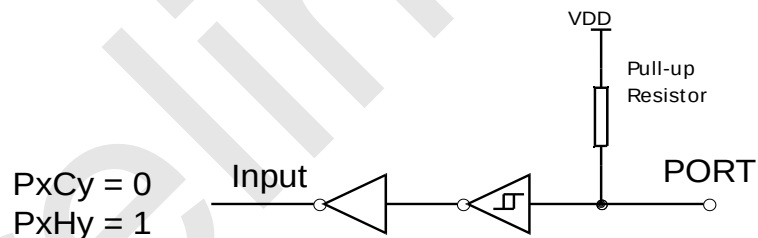


Strong push-pull output mode

9.3.2 Input mode with pull-up

In the input mode with Pull-up, a pull-up resistor is permanently connected to the input port; a low-level signal is detected only when the input port voltage is pulled down.

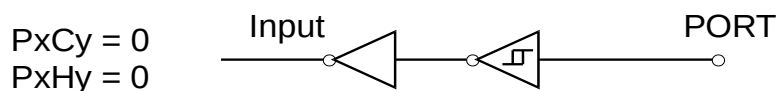
The port structure diagram for the input mode with Pull-up is shown below:



Input mode with pull-up

9.3.3 High impedance input mode (input only)

The port structure diagram for High Impedance Input Mode is shown below:



High impedance input mode

10 Analog-to-digital converter (ADC)

10.1 Clock source

- The ADC clock source for the SC32F11T/11G Series is a single source: PCLK2
- ADC conversion time is approximately 950 ns

10.2 Feature

- Precision: 14-bit
- Supports up to 20 channels: 18 external ADC sampling channels plus other IO port functions multiplexed
 - One Internal ADC Channel can directly measure V_{DD} Voltage
 - One Internal ADC Channel can directly measure OP output
- Built-in 2.4 V, 2.048 V, and 1.024 V reference voltages
- The ADC offers four reference voltage options: V_{DD} , 2.4 V, 2.048 V, and 1.024 V
- ADC Input Channel Selection
 - Select the ADC input channel by setting the ADCIS[4:0] bits.
- Conversion can be started through software
- ADC Conversion Completion Interrupt can be enabled
- The total time from sampling to conversion completion is as low as 2 μ s
- Supports DMA transfer: a DMA Request is generated upon ADC conversion completion
- Supports Single Channel Continuous Conversion Mode
- ADC conversion results support Overflow Flag indication; the OVERRUN Flag shares the same ADCV Register with the conversion results, allowing users to read them simultaneously.

10.3 ADC conversion steps

The steps users need to follow for performing ADC conversion are as follows:

1. Configure the ADC input Pin; (Configure the bit corresponding to AINx as an ADC input, usually ADC Pins are preset)
2. Set the ADC Reference Voltage V_{ref} and the frequency for ADC Conversion
3. Write 1 to ADCEN to Enable the ADC module Power Supply
4. Select the ADC Input Channel by setting the ADCIS bit
5. Start ADCS to begin Conversion
6. Wait until ADCIF=1. If ADC Interrupts are Enabled, an ADC Interrupt will be generated, and the user must clear the ADCIF Flag in software
7. Obtain 14-bit data from ADCV after each conversion is completed
8. If not changing the input channel, set CONT to 1 in software to Enable Single Channel Continuous Conversion Mode. Conversion continues until this bit is cleared.
9. When ADC conversion results overflow, the OVERRUN Flag is set to 1.
10. Conversion data can be transferred via DMA.

Note: Before setting ADC_CON[8] (INTEN), users should clear ADCIF in software first and also clear

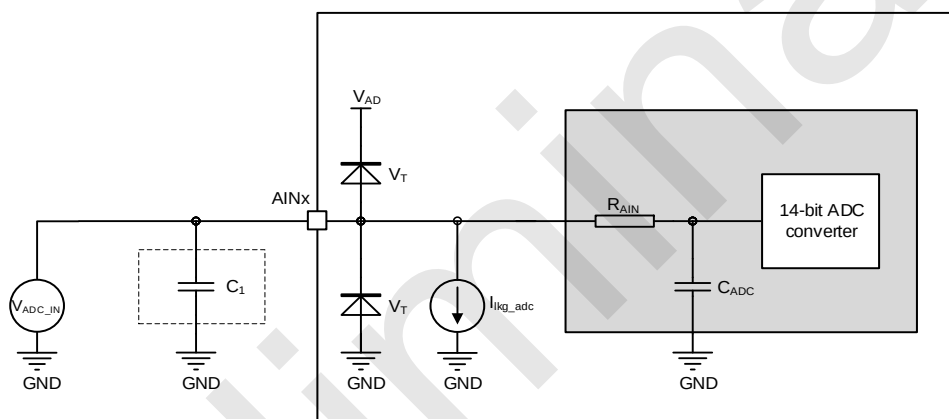
ADCIF at the end of the ADC Interrupt Service Routine to prevent continuous ADC Interrupts.

10.4 ADC interrupts

After ADC conversion completion in the SC32F11T/11G Series, ADCIF will be set. If ADC_CON.INTEN=1, an interrupt will be generated.

Interrupt Event	Event Flag	Interrupt Enable Control Bit
ADC Conversion Complete Interrupt Request	ADCIF	ADC_CON->INTEN

10.5 ADC connection circuit diagram



Description:

- C_1 is an external $0.01\mu F$ capacitor; it is recommended that users add this capacitor to enhance ADC performance.
- For ADC related electrical characteristics, see section [27.10 ADC Electrical Characteristics](#).

11 Operational amplifier and programmable gain amplifier (OP)

A built-in OP integrates an operational amplifier and a Programmable Gain Amplifier, providing rail-to-rail operation. The OP can be configured as PGA Mode, featuring 5 Non-inverting Inputs, 2 Inverting Inputs, and 3 Outputs, and supports non-inverting gains of 8, 16, 32, or 64 times and inverting gains of 7, 15, 31, or 63 times.

11.1 Feature

- One Rail-to-Rail Operational Amplifier
- Configurable as PGA Mode
 - Non-inverting Input Gain: 8/16/32/64
 - Inverting Input Gain: 7/15/31/63
- Non-inverting Input routed to two external Pins: OP_P0 or OP_P1
- Inverting Input routed to one external Pin: OP_N
- An external pin is output at the output terminal: OP_O
- The output can be directly connected to the ADC input
- The output can be directly connected to the positive input of CMP
- Precision adjustment can be achieved by setting the PGA input offset control bit PGAOFC=1, connecting the OP module's non-inverting input and inverting input together.

11.2 OP port selection

11.2.1 OP non-inverting input selection

The OP Module has five types of non-inverting inputs: OP_P0 external pin, OP_P1 external pin, internal V_{SS} , internal 1.2 V reference, and V_{DD} ; these can be selected via OPPSEL[2:0].

11.2.2 OP inverting input selection

The OP module's inverting input has two options: OP_N external Pin and internal feedback resistor.

- When selecting the OP_N external Pin as the OP's inverting input, set the OP input control bit OPNSEL=0 and the feedback resistor connection selection bits FDBRSEL[1:0]=01.
- When selecting the internal feedback resistor as the OP's inverting input, set OPNSEL=1, FDBRSEL[1:0]=00, 11, or 10, and choose the internal gain stage via the PGAGAN[1:0] bits.

11.2.3 OP output selection

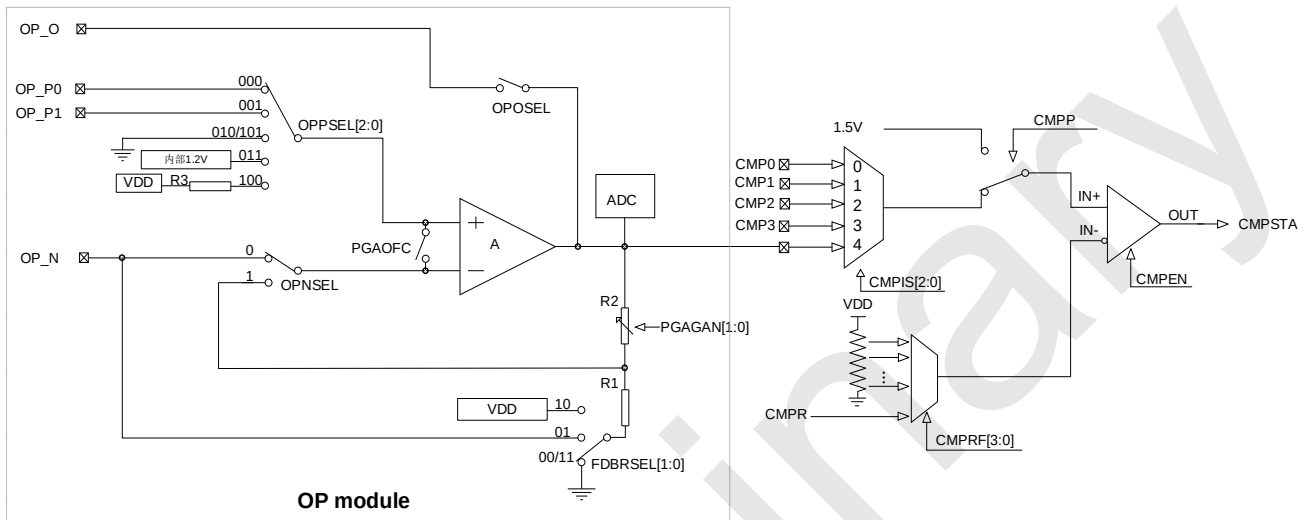
The OP module has three outputs: three pins corresponding to the AD converter sampling channel, the positive input of the CMP, and the OP_O pin.

When the OP output is used as the analog input for the AD converter or the positive analog input of CMP0, configure it as follows:

- To use the OP as the ADC input, first enable the OP module by setting ENOP=1, then enable the ADC power supply by setting ADCEN=1, and select the OP output as the ADC input via ADCIS[4:0]. The OP conversion result can then be read directly from the ADCV register.

- When OP is used as the positive input of the CMP, and OP is enabled, if the CMP input channel control bits CMPIS[2:0] are set to OP, then the CMP's positive input is selected from the OP output.

11.3 Block diagram of the OP circuit structure



12 Analog comparator (CMP)

The SC32F11T/11G Series integrates an analog comparator (CMP), and CMP interrupts can wake the device from STOP Mode. It can be applied to alarm circuits, power supply voltage monitoring circuits, zero-cross detection circuits, and similar applications.

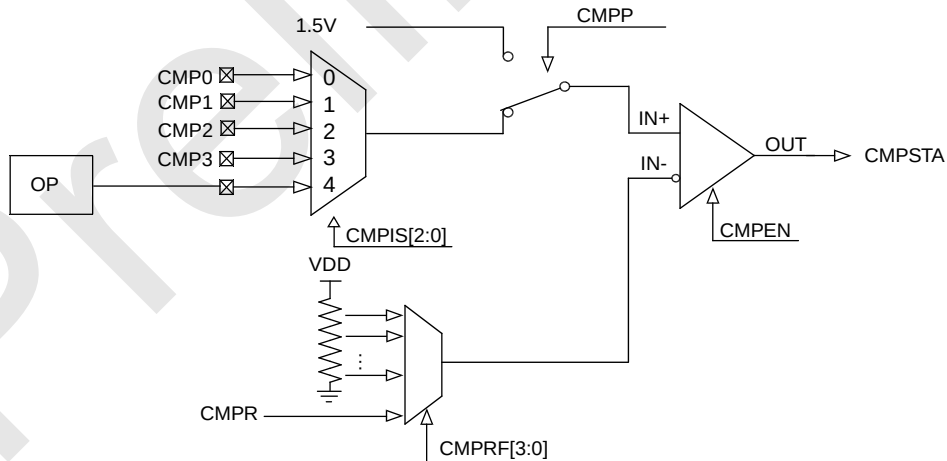
This comparator has five analog positive input terminals: CMP0 through CMP3, and the OP output terminal, selectable via CMPIS[2:0]. The negative input voltage can be switched by CMPRF[3:0] to either the external voltage at the CMPP pin or one of the 15 internal reference voltages.

The comparator interrupt mode can be conveniently set via CMPIM[1:0]. When the interrupt condition defined by CMPIM[1:0] occurs, the comparator interrupt flag CMPIF is set to 1 and must be cleared by software.

12.1 Feature

- Positive input signal selectable from five options:
 - Four analog signal positive input pins CMP0 to CMP3
 - OP output terminal
- Negative input voltage can be selected from the CMPP pin or one of the 15 internal V_{DD} voltage division comparison voltages
- CMP Interrupts can wake up STOP Mode

12.2 Analog comparator block diagram



Analog comparator block diagram

13 UART0 to 5

13.1 Clock source

- All UARTs in the SC32F11T/11G Series share a single clock source derived from PCLK.

13.2 Feature

- 6 UARTs: UART0 through UART5
- UART0 to UART5 support signal port remapping, allowing mapping to an alternate set of IO pins.
- Independent Baud Rate Generator
- Four selectable communication modes:
 - SM0 and SM1 Serial Communication Mode Control Bits
 - Mode 0: 8-bit half-duplex synchronous communication mode, transmitting and receiving serial data on the RXD pin. The TXD pin serves as the transmit shift clock. Each frame consists of 8 bits, with the least significant bit transmitted or received first
 - Mode 1: 10-bit full-duplex Asynchronous Communication, consisting of 1 Start bit, 8 data bits, and 1 Stop bit, with variable communication Baud Rate.
 - Mode 2: Reserved
 - Mode 3: 11-bit full-duplex Asynchronous Communication, consisting of 1 Start bit, 8 data bits, one programmable 9th bit, and 1 Stop bit, with variable communication Baud Rate.
- Transmit and Receive completion can generate Interrupts and set the corresponding flags TXIF and RXIF; Interrupt Flags must be cleared by software.
- UART0 and UART1 can generate DMA Requests.
- UART2 to 5 cannot generate DMA Requests.
- Independent Baud Rate Generator
- UART0/1/2/3/4/5 support Wake up from STOP Mode:
 - START bit Falling Edge can Wake up STOP Mode.
 - Provides wake up Interrupt Enable bit WKIE and wake up Interrupt Flag WKIF

14 QSPI0 to 1

14.1 Clock source

The SPI clock source in the SC32F11T/11G Series is single and derived from PCLK.

14.2 QSPI0/1 feature

- QSPI Supports Master Mode Only
- Each QSPI supports four transfer widths: 8, 16, 24, and 32 bits, with a fixed 8-level FIFO for each width, and independent transmit and receive.
- Supports Single-, Dual-, and Quad-Wire Communication
- Supports two functional modes: QSPI half-duplex communication mode and pass-through mode
- Communication speed up to 32 Mbps
- Both QSPI units can perform direct pass-through without FIFO
- Supports DMA

15 SPI0 to 3

The SC32F11T/11G features up to four SPI ports: SPI0/1 are from the advanced two in one interface, and SPI2/3 are from the general two in one interface. SPI0/1 have 8-level FIFO, whereas SPI2/3 have no FIFO. In SPI communication mode, the output drive capability of SPI0/1 signal pins is enhanced, while SPI2/3 does not support this feature.

15.1 Clock source

- The SPI clock source in the SC32F11T/11G Series is single and derived from PCLK.

15.2 SPI0/1 feature

- Supports 13-level SPI clock prescaling, enabling the user to set a lower frequency.
- SPI0/1 Signal Pin Strong Drive:
 - In SPI communication mode, the output drive capability of the corresponding signal pins is enhanced; in other modes, it matches standard IO characteristics.
- Equipped with an 8-level FIFO buffer, with independent Transmit and Receive.
 - The FIFO function of SPI0/1 allows continuous writing of up to 8 pieces of 8/16/24/32-bit data into the SPI transmit buffer (SPI0/1_DATA). During transmission, data written first is transmitted first. When the data written by the user into the FIFO is completely transmitted, the transmit FIFO empty flag TXEIF is set to 1. If the FIFO is full, the write collision flag WCOL is set, preventing the user from writing data into the FIFO until data inside the FIFO is transmitted and space is available. The interrupt flag QTWIF is set once after each frame of data is transmitted.
 - When continuously reading up to 8 units of 8/16/24/32-bit data from the SPI receive buffer (SPI0/1_DATA), the earliest received data is read first.
 - Half FIFO data transfer interrupts and their corresponding flags are provided to help users read or write data in a timely manner:
 - ◆ An interrupt and corresponding flag TXHIF are provided for when valid transmit FIFO data is less than half full.
 - ◆ Provides interrupt when receive FIFO is more than half full and the corresponding flag RXHIF
 - Supports receive buffer overflow interrupt and the corresponding flag to promptly notify exceptions
- Supports Master and Slave Mode
- Supports DMA
 - Enable TXDMAEN; after the transmit buffer empty flag TXEIF is set, a DMA request can be triggered. After DMA writes to the transmit buffer, the TXEIF flag is automatically cleared
 - Enable RXDMAEN; after the receive buffer non-empty flag RXNEIF is set, a DMA request can be triggered. After DMA reads from the receive buffer, the RXNEIF flag is automatically cleared

15.3 SPI2/3 features

- Supports 13-level SPI clock prescaling, enabling the user to set a lower frequency.
- Signal pins can be mapped to three other IO groups
- No FIFO

- Supports Master and Slave Mode
- Supports DMA
 - SPI2 can generate DMA requests
 - SPI3 cannot generate DMA requests

15.4 Comparison between SPI0/1 and SPI2/3

Comparison BIT	SPI0/1	SPI2/3
Strong drive on signal pin	Available	None
WCOL	When the transmit FIFO is full, writing to it is not possible; WCOL will be set, indicating a buffer write collision.	While a frame is being transmitted, writing to the transmit buffer is prohibited; WCOL will be set, indicating a buffer write collision.
QWIF	From this bit onwards, it indicates the completion of a frame's data reception/transmission.	From this bit onwards, it indicates the completion of a frame's data reception/transmission.
QWIE	QWIF interrupt enable bit set	None
RXHIE	Interrupt enable bit for receive FIFO exceeding half full	None
TXHIE	Interrupt enable bit for transmit FIFO less than half full	None
RXIE	Interrupt enable bit for receive FIFO full	None
TBIE	Interrupt enable bit for transmit FIFO empty	Interrupt enable bit for transmit buffer empty
RXNEIE	Interrupt enable bit for receive FIFO non-empty	None
RXHIF	Starting at this bit position, indicates valid data in the receive FIFO exceeds half full.	None
TXHIF	Starting at this bit position, indicates valid data in the transmit FIFO is less than half full.	None
RXFIF	Starting at this bit position, indicates the receive FIFO is full.	None
TXEIF	Starting at this bit position, indicates the transmit FIFO is empty.	Starting at this bit position, indicates the transmit buffer is empty.
RXNEIF	Receive FIFO non-empty flag	None
DMA	DMA requests are triggered by the transmit buffer empty flag TXEIF and the receive buffer non-empty status bit RXNEIF.	SPI2: Frame-end unified set request SPI3: DMA not supported

16 TWI0 to 3

16.1 Clock source

- TWI clock source of the SC32F11T/11G Series is only from PCLK.

16.2 TWI0/1 features

- Shares register addresses and signal pins with QSPI0/1 and SPI0/1, but functions are completely independent.
- Supports 11-level TWI clock prescaler; in Master Mode, the TWI communication rate defaults to the minimum prescale level ($f_{PCLK}/4$).
- Configurable for Master Mode or Slave Mode
- Bidirectional data transfer between Master and Slave
- Communication rate up to 1 Mbps
- Optional clock stretching
- Supports DMA
 - Both TWI0 and TWI1 can generate DMA requests

16.3 Features of TWI2 and TWI3

- Shares register addresses and signal pins with SPI2 and SPI3 but operates completely independently
- Supports 11-level TWI clock prescaler; in Master Mode, the TWI communication rate defaults to the minimum prescale level ($f_{PCLK}/4$).
- Three selectable signal pin mapping groups
- Configurable for Master Mode or Slave Mode
- Bidirectional data transfer between Master and Slave
- Communication rate up to 1 Mbps
- Optional clock stretching
- Supports DMA
 - TWI2 can generate DMA requests
 - TWI3 cannot generate DMA Request

16.4 TWI signal description

On the TWI Bus, data is transferred synchronously byte by byte between the Master and Slave devices via the clock line SCL and the data line SDA. Each data byte consists of 8 bits; one SCL clock pulse transmits one data bit, starting with the most significant bit (MSB). After each byte, an acknowledgment bit follows. Each bit is sampled when SCL is high. Therefore, the SDA line may change while SCL is low but must remain stable when SCL is high. When SCL is high, transitions on the SDA line are interpreted as commands (START or STOP).

- TWI Clock Signal Line (SCL)

This clock signal is generated by the Master and connected to all Slave devices. One data byte is transferred

every 9 clock periods. The first 8 cycles are used for data transmission, and the last clock serves as the acknowledgment clock from the receiver. The idle state should be at a logic high level, pulled up by the pull-up resistor on the SCL line.

- TWI data signal line (SDA)

SDA is a bidirectional signal line, and the idle state should be at a logic high level, pulled up by the pull-up resistor on the SDA line.

Preliminary

17 CAN communication port

17.1 Overview

The Controller Area Network (CAN) in the SC32F11T/11G Series supports communication protocols CAN2.0B and CAN_FD. Compared to CAN2.0B, CAN_FD offers greater flexibility with a variable bit rate—originally fixed at 1 Mbit/s—and supports data segments up to 64 bytes in length. Supports four different working modes, including configurable low power standby mode, and supports wake up from standby.

The transmit buffer provides two options: PTB Primary Transmission Buffer and STB Secondary Transmission Buffer. Transmission order can be determined using either FIFO mode or priority mode. The receive buffer can store 8 frames simultaneously, with each received frame having its own time-stamp. There are 8 groups of receive filters available; each filter can be enabled independently and configured with filtering conditions.

17.2 Clock source

AHB clock bus, with the clock source following HCLK.

17.3 Feature

- Protocol Support:
 - CAN 2.0B
 - ◆ Supports standard and extended formats, with a maximum payload of 8 bytes.
 - ◆ Supports data rates up to 1 Mbit/s.
 - CAN FD
 - ◆ Supports standard and extended formats, with a maximum payload of 64 bytes.
- Variable Rate
- Standby Mode: When enabled, the CAN transceiver enters a low power state, stops receiving data frames, and only detects dominant levels on the CAN bus.
- Time-Stamping:
 - CiA 603: 64-bit time-stamping; transmit frames (TTS) have a single time-stamp stored in a register, while every receive frame (RTS) has its own individual time-stamp.
- Transmit and Receive Buffers
 - The message buffer area is located in the SRAM, and the address can be configured
 - 8 Receive Buffers (RB); each receive frame (RTS) has a separate time-stamp stored together with the data in the RB. The RB operates as a FIFO.
 - 9 Transmit Buffers (TB):
 - ◆ 1 Primary Transmit Buffer (PTB)
 - ◆ 8 Secondary Transmit Buffers (STB), supporting two transmission modes: FIFO mode and priority-based mode.
 - 8 Receive Filters (supports 29-bit ID)

18 Hardware watchdog WDT

The SC32F11T/11G Series features a built-in hardware Watchdog WDT, with its clock source being an internal 37 kHz oscillator. Users can enable or disable the Watchdog Reset function via the ENWDT control bit in the Customer Option of the programmer.

The hardware Watchdog WDT offers high security, precise timing, and flexible usage. This Watchdog peripheral can detect faults caused by software errors and triggers a System Reset when the counter reaches the set overflow time.

The WDT is driven by its internal low-frequency oscillator, ensuring it remains operational even if the main clock fails.

18.1 Clock source

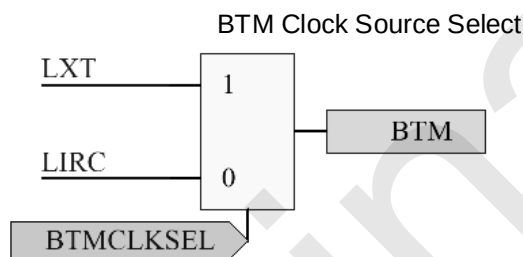
The clock source of the WDT in the SC32F11T/11G Series is fixed to LIRC. Once the WDT is enabled, LIRC automatically starts and remains oscillating throughout the WDT operation; users cannot disable it.

19 Base timer (BTM)

The SC32F11T/11G Series has a built-in Base Timer (BTM) that can generate Interrupts at intervals ranging from 15.625 ms to 32 s. Both the 37 kHz LIRC and the external 32.768 kHz Crystal Oscillator LXT can be used as the Clock Source for the BTM. Interrupts generated by the BTM can wake the CPU from STOP mode.

19.1 Clock source

- The BTM clock source options for the SC32F11T/11G Series include LXT and LIRC.



19.2 Feature

- Interrupt frequency interval selectable between 15.625 ms and 32 s
- Wakeup STOP Mode

20 Built-in CRC verification module

The SC32F11T/11G Series features a built-in CRC Verification Module that uses a polynomial generator to produce CRC codes from 8-bit, 16-bit, or 32-bit data Words.

20.1 Clock source

- The CRC clock source of the SC32F11T/11G Series is derived from HCLK

20.2 Feature

- Built-in hardware CRC module
- Initial value configurable, default is 0xFFFFFFFF
- Supports 8-bit, 16-bit, and 32-bit data units
- Polynomial is programmable, default is 0x04C1_1DB7
- Only supports software mode for data input calculation
- Supports DMA: CRC_DR can be used as a DMA target Address and can also be accessed directly via Register
- CRC calculation for a single byte requires 1 system Clock.

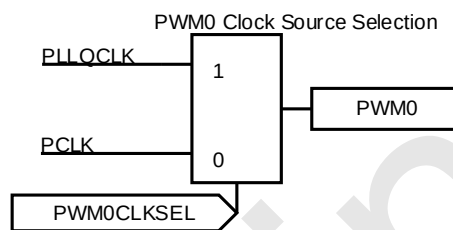
CRC algorithm name	CRC-32/MPEG-2
Polynomial formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Data width	32bit
Initial value	0xFFFFFFFF
Result XOR value	0x00000000
Input value inversion	false
Output Inversion	false
LSB/MSB	MSB

Note: The data written to and read from CRCDR are not the same.

21 PWM0: 8-channel 16-bit multifunction PWM

21.1 Clock source

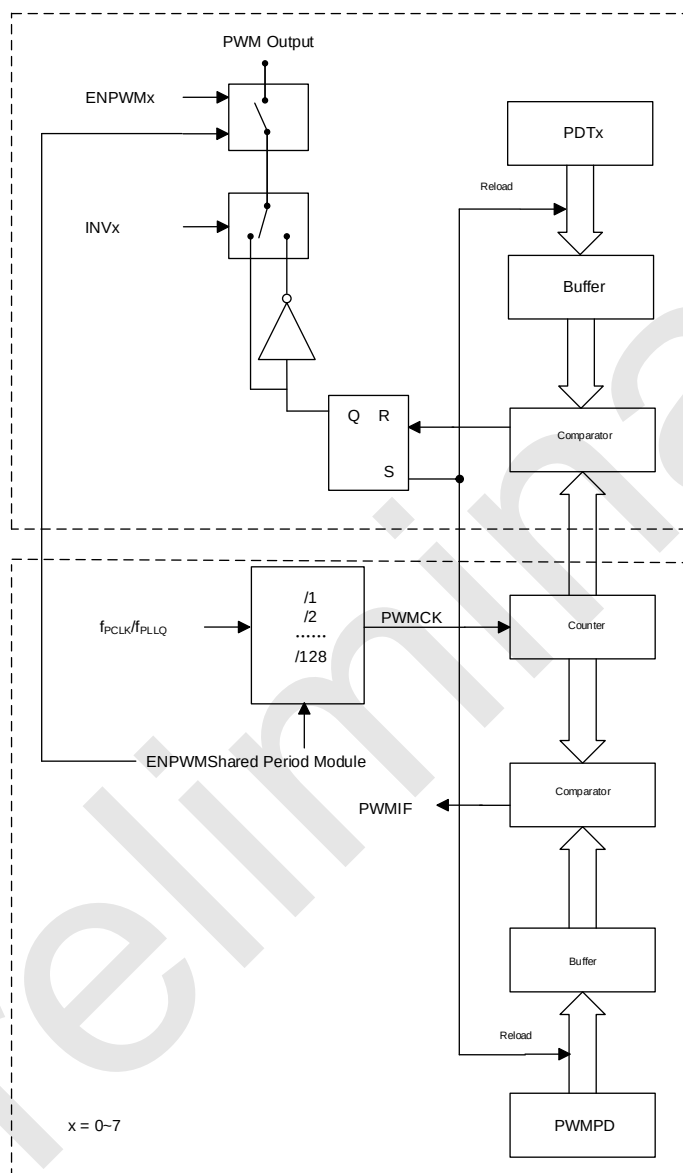
- The clock source of the SC32F11T/11G Series PWM0 can be selected between PLLQCLK and PCLK
- PWM0 output frequency can reach the frequency of the selected clock source
- PWM0 clock prescaler range: /1 to /128



21.2 Feature

- Supports 8-stage PWM0 clock prescaling
- 8-channel 16-bit common-period multifunction PWM
- Output waveform can be inverted
- Waveform type: can be set to center-aligned or edge-aligned
- PWM Mode: can be set to independent mode or complementary mode
 - In independent mode, the 8 PWM channels share the same period, but each channel's on-time and output waveform duty cycle can be adjusted individually.
 - In complementary Mode, four groups of complementary PWM waveforms with Dead Time can be output simultaneously.
- Provides one PWM overflow Interrupt
- Supports Fault Detection mechanism
- Has independent Interrupt request Flags

21.3 PWM0 block diagram



PWM0 block diagram

21.4 PWM0 general configuration

21.4.1 Output mode

- In independent Mode, 8 PWM channels share the same Period, but each PWM output waveform's Duty Cycle can be set individually.
- In complementary Mode, four groups of synchronous, complementary PWM waveforms with Dead Time can be output simultaneously.

21.4.2 Alignment type

- Edge-aligned
- Center-aligned

21.4.3 Duty cycle variation feature

When PWM0n outputs a waveform, the Duty Cycle can be changed by modifying the value of the high-level setting Register (PDT0x). Note that when changing the value of PDT0x, the duty cycle does not change immediately; it updates only when the PWM counter reaches 0 or counts up to match the period setting PWMPD[15:0] + 1.

21.4.4 Period change feature

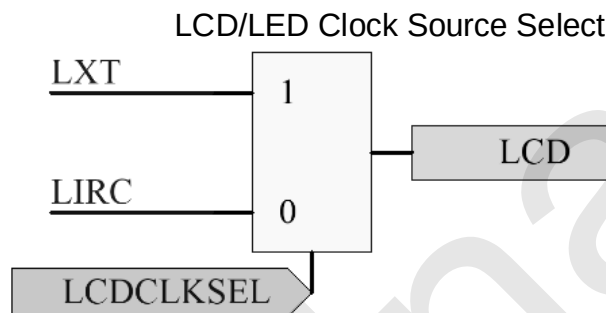
When the PWM output waveform is active, you can change the period by modifying the value of the period setting register PWMPD. Changing the value of PWMPD does not immediately affect the period; the change takes effect only when the PWM counter reaches 0 or counts up to match the period setting PWMPD[15:0] + 1.

22 LCD/LED driver

- LCD/LED selectable, sharing registers and IO ports.

22.1 Clock source

- The SC32F11T/11G Series LCD/LED supports two clock sources: LXT and LIRC.



22.2 Built-in 8 COM x 31 SEG LED driver

- Voltage driving method with 1/1 to 1/8 duty cycle
- Software-supportable switching between common cathode and common anode modes

22.3 Built-in 8 COM x 31 SEG LCD driver

- Selectable Type A / Type B waveform
- 8 x 31, 6 x 33, 5 x 34, or 4 x 35
- Selectable voltage division resistor at LCD voltage output port
- LCD display driving bias voltage
 - 1/4 bias voltage
 - 1/3 bias voltage
- Three selectable frame frequencies:
 - 32/64/128 Hz in Type A mode
 - 64/128/256 Hz in Type B mode

23 42-channel high sensitivity touch circuit (TK)

- High sensitivity mode
- Suitable for capacitive proximity keys, proximity sensing, and other touch applications requiring high sensitivity
- Channels can be scanned in parallel
- CMOD pin requires a 103 capacitor connected to ground
- Supports self-capacitance and mutual-capacitance modes
- The TK internal reference voltage maximum setting can be set to 4 V to achieve higher sensitivity.
- Supports low power mode
- Supports fast wake up from STOP Mode
- Complete development support: highly flexible touch software library and intelligent debug software

Note: Only the SC32F11T series supports the TK function.

24 16-bit timers/counters (TIM) Timer0 to Timer7

24.1 Clock source

- In timer mode/PWM output mode, the TIM clock source is derived from PCLK.
- In counter mode, the Tn pin serves as the count source input.

24.2 Feature

- 8 independent 16-bit auto-reload counters Timer0 to Timer7
- 16-bit upcounting, downcounting, and up/down auto-reload counters
- Supports rising edge/falling edge capture, enabling PWM duty cycle and period capture
- 16-bit programmable prescaler, with division factor of the counter clock frequency adjustable between 1 and 65535
- Overflow and capture events of TIM1/2/6 can generate DMA requests
- TIM2 to 7 Tn/TnCAP/TnPWMA pins support remapping and can be assigned to a different group of IO pins.

24.3 Counting method

24.3.1 TIM counting method in timer mode

- Count up: counts up from the set value to 0xFFFF before overflowing.
- Count down: counts down from 0xFFFF to the set value.

24.3.2 TIM counting method in PWM output mode

Only count up is allowed in PWM output mode: counting starts from 0 and counts up; when reaching the duty cycle setting PDT, the PWM output waveform switches between high and low levels, then continues counting up to the set reload value RLD, at which point it overflows and restarts counting from 0.

The PWM output period T from TIM_{PWM} is calculated by the following formula:

$$T_{PWM} = \frac{RLD[15:0] + 1}{PCLK}$$

Duty cycle calculation formula:

$$duty = \frac{PDT[15:0]}{RLD[15:0] + 1}$$

24.4 Timer-related signal pins

- TnCAP/Tn, n=0 to 7
 - Tn clock input/output
 - TnCAP can capture on both Rising Edge and Falling Edge

Note: Tn and TnCAP are multiplexed functions and cannot be used simultaneously.

- TnEX, n=0 to 7
 - In reload mode, the external event input on the TnEX pin (Falling Edge) is used to control reload enable or disable.
 - In capture mode, when FSEL = 1, the TnEX pin acts as a Falling Edge capture signal input. Upon detecting a falling edge on TnEX, a capture event occurs, EXIF is set, and the value in the TnCNT register is stored in the FCAP register.
- TnPWM, n=0 to 7
 - Each TIM channel can provide two PWM signals with the same Period via the Tn and TnEX ports, each having independently adjustable duty cycles: TnPWMA and TnPWMB.
 - TnPWMA and TnPWMB share the same Period, and their clock source follows the TIM.

Note: The PWM Capture and PWM Output functions of TIM cannot be enabled simultaneously.

24.5 TIM interrupts and their corresponding flags

- Counter overflow/underflow share the interrupt flag TIF.
- Capture Status Flags:
 - EXIF flag indicates a falling edge has been detected on the external event input.
 - EXIR flag indicates a rising edge has been detected on the external event input.
- Interrupt and Priority Configuration Control Bits are integrated into the NVIC module.

24.6 TIM operating modes

- Mode 0: 16-bit Capture Mode, supporting PWM Both Edge Capture.
- Mode 1: 16-bit auto-reload Timer/Counter mode.
- Mode 3: Programmable Clock Output mode.
- Mode 4: PWM output mode.

25 DMA controller

25.1 Overview

The Direct Memory Access (DMA) controller is used for high-speed data transfer. The DMA controller can transfer data from one address to another without CPU intervention. Data transfer via DMA reduces the CPU workload, allowing the saved CPU resources to be used for other applications. The DMA controller contains 4 channels, each directly connected to dedicated hardware DMA requests, and each channel also supports software triggering. The DMA controller supports 4 levels of channel priority for managing DMA request priorities, ensuring that only one DMA channel operates at any given time. The DMA controller also supports single and burst transfers; the request source can be either a software request or an interface request. Data transfer between memories uses software requests.

Note: For bidirectional data transfer applications, two DMA channels are required to separately perform transmitting and receiving.

25.2 Clock source

The DMA clock source is HCLK, and the peripheral clock for DMA is enabled via AHB_CFG.DMAEN.

25.3 Feature

- Supports 4 independently configurable channels
- Supports four request priorities
- Supports 8-bit, 16-bit, and 32-bit data transfers
- Supports source and destination address auto-increment or fixed addressing, with data widths supporting byte, half-word, and word
- Supports single and burst transfer modes.

25.4 Function description

25.4.1 Transfer direction

Memory to Memory	Memory to Peripheral	Peripheral to Memory	Peripheral to Peripheral
Unlimited	Unlimited	Unlimited	Unlimited

25.4.2 DMA access region restriction

When users operate DMA, writing to Flash is prohibited, and operating the Core via DMA is also not allowed; otherwise, unpredictable exceptions may occur.

25.4.3 Channel priority

Four priority levels can be set via register PL[1:0]:

- 00: Low
- 01: Medium
- 10: High
- 11: Very High

25.4.4 Single transfer and burst transfer

The DMA controller supports single and burst transfer modes. Request sources can be software or interface requests. Data transfers between Memory regions use software requests. Single transfer means the software or interface prepares to transfer one data unit (each data requires one request). Burst transfer means multiple data units are transferred with only one request.

Single Transfer and Burst Transfer modes can be configured via the register TPTYPE (DMA_n_CFG[15]).

When the DMA controller operates in Single Transfer mode, each data movement requires one request; each time data is moved, the register DMA_n_CNT[31:0], n=0 to 3, decreases by 1 until the count in DMA_n_CNT[31:0] reaches 0, at which point the transfer completes. In this mode, BURSIZE (DMA_n_CFG[14:12]) does not control the amount of data transferred; its value is fixed at 1.

In Burst Transfer mode, the DMA controller transfers DMA_n_CNT[31:0] data items with a single request. After transferring BURSIZE data (DMA_n_CFG[14:12]), the value in DMA_n_CNT[31:0] decreases by BURSIZE. The data transfer is complete only when the value in DMA_n_CNT[31:0] decreases to zero.

25.5 Loop mode

Loop Mode can be used to handle circular buffers and continuous data streams (such as ADC scan mode). During transmission in Loop Mode, the number of data items to be transferred is automatically reloaded to the initial value set during channel configuration, and DMA requests continue to be serviced. To stop loop transmission, software must first stop the peripheral from generating DMA requests (for example, exit ADC scan mode) before disabling the DMA channel. Software must explicitly set the DMACNT value both before starting/enabling transmission and after stopping loop transmission.

The DMA controller of the SC32F11T/11G Series supports Normal Mode and Loop Mode:

- When CIRC=0 (the DMA channel operates in non-loop mode), no further DMA requests will be accepted after the programmed number of data items to be transferred is reached
- When CIRC=1 (DMA channel is in Loop Mode), after the transfer completes, the channel's DMACNT will automatically reload the previously set value, waiting for the next loop.

Users can choose flexibly according to their actual needs.

26 SysTick

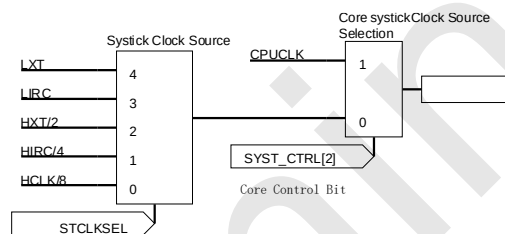
SysTick is a simple, 24-bit write-to-clear, decrementing, auto-reload counter with a flexible control mechanism. This counter can be used as the tick timer for a real-time operating system (RTOS) or as a simple counter.

26.1 Clock source

The clock sources of SysTick (Cortex®-M0+ Core SysTick) are divided into internal and external clock sources:

- The internal clock source is the CPU clock.
- There are five external clock sources.

The block diagram of the SysTick clock sources is as follows:



26.2 SysTick calibration register default value

The method for setting the calibration value of the SysTick Calibration Register is as follows:

- If the default power-on clock is f_{HCLK}/n (MHz), where n is the default power-on divider factor, and the default power-on Clock Source is HIRC
- Then the initial SysTick calibration value is $1000 \cdot (f_{HCLK}/n)$, which ensures the default can generate a 1 ms time base.

27 Electrical characteristics

Unless otherwise specified, the electrical data in this chapter are based on the operating conditions listed in the [Recommended Operating Conditions](#) section.

27.1 Recommended operating conditions

Symbol	Parameter	Minimum Value	Maximum Value	Unit	System Clock Frequency
V _{DD}	Operating Voltage	2.0	5.5	V	32 MHz
T _A	Ambient Temperature	-40	105	°C	

27.2 Absolute maximum ratings

Symbol	Parameter	Minimum Value	Maximum Value	Unit
V _{DD}	DC supply voltage	-0.3	6	V
V _{PIN}	Input/output voltage of any pin	-0.3	V _{DD} +0.3	V
T _A	Ambient Temperature	-40	105	°C
T _{STG}	Storage temperature	-55	125	°C
I _{VDD}	Current flowing through V _{DD}	-	250	mA
I _{VSS}	Current flowing through V _{SS}	-	250	mA

27.3 Flash ROM parameters

(V_{DD} = 5 V, T_A = +25 °C, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
N _{END}	APROM Endurance (erase/write cycles)	100,000	-	-	Cycles	Clock Source: HIRC
T _{DR}	Data retention time	10	-	-	Years	
T _{S-Erase}	Single sector erase time	-	2.5	-	ms	
T _{Erase}	Page erase time	30	-	40	ms	
T _{Write}	Single byte write time	-	30	-	μs	

27.4 Power consumption

27.4.1 $V_{DD} = 5\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$, booting from APROM unless otherwise specified

Symbol	Parameter	Boot Area	Minimum Value	Typical values	Maximum Value	Unit	Condition
I_{op1}	Operating current	APROM	-	9	-	mA	$f_{HCLK} = 64\text{ MHz}$ Clock Source: HIRC
			-	6	-	mA	$f_{HCLK} = 32\text{ MHz}$ Clock Source: HIRC
			-	3.5	-	mA	$f_{HCLK} = 16\text{ MHz}$ Clock Source: HIRC
			-	2.5	-	mA	$f_{HCLK} = 8\text{ MHz}$ Clock Source: HIRC
			-	2.0	-	mA	$f_{HCLK} = 4\text{ MHz}$ Clock Source: HIRC
			-	1.6	-	mA	$f_{HCLK} = 2\text{ MHz}$ Clock Source: HIRC
I_{pd1}	Standby Current (Power Down Mode)	APROM	-	2.6	-	μA	$f_{HCLK} = 32\text{ MHz}$ Clock Source: HIRC
I_{IDL1}	Standby Current (Idle Mode)	APROM	-	1.7	-	mA	$f_{HCLK} = 32\text{ MHz}$ Clock Source: HIRC

27.4.2 $V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$, boot from APROM unless otherwise specified

Symbol	Parameter	Boot Area	Minimum Value	Typical values	Maximum Value	Unit	Condition
I_{op1}	Operating current	APROM	-	9	-	mA	$f_{HCLK} = 64\text{ MHz}$ Clock Source: HIRC
			-	6	-	mA	$f_{HCLK} = 32\text{ MHz}$ Clock Source: HIRC
			-	3.5	-	mA	$f_{HCLK} = 16\text{ MHz}$ Clock Source: HIRC
			-	2.5	-	mA	$f_{HCLK} = 8\text{ MHz}$ Clock Source: HIRC
			-	2.0	-	mA	$f_{HCLK} = 4\text{ MHz}$ Clock Source: HIRC
			-	1.5	-	mA	$f_{HCLK} = 2\text{ MHz}$ Clock Source: HIRC
I_{pd1}	Standby Current (Power Down Mode)	APROM	-	2.4	6	μA	$f_{HCLK} = 32\text{ MHz}$ Clock Source: HIRC
I_{IDL1}	Standby Current (Idle Mode)	APROM	-	1.7	6	mA	$f_{HCLK} = 32\text{ MHz}$ Clock Source: HIRC

27.5 GPIO parameter

27.5.1 $V_{DD} = 5\text{ V}$; $T_A = +25\text{ }^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
V_{IH1}	Input high voltage	$0.7 V_{DD}$	-	$V_{DD}+0.3$	V	
V_{IL1}	Input low voltage	-0.3	-	$0.3 V_{DD}$	V	
V_{IH2}	Input high voltage	$0.8 V_{DD}$	-	V_{DD}	V	Schmitt Trigger Input:

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
V_{IL2}	Input low voltage	-0.2	-	$0.2 V_{DD}$	V	NRST T_CLK / T_DIO UART0 to 5 RXD Input SPI / TWI Signal Input INT0 to INT15 PWM Fault Detection Input FLT Timer Clock Input Tn Timer Capture Input TnEX
I_{OL1}	Standard Drive Capability IO Group Output low current	-	30	-	mA	$V_{Pin} = 0.4 V$
		-	55	-	mA	$V_{Pin} = 0.8 V$
I_{OL2}	COM port IO group Output low current	-	60	-	mA	$V_{Pin} = 0.4 V$
		-	100	-	mA	$V_{Pin} = 0.8 V$
$I_{OHQSPIA}$	QSPI0/1 signal pins (only when QSPI is enabled): QSPI0/1IO0 QSPI0/1IO1 QSPI0/1IO2 QSPI0/1IO3 SCK0/1 Output high current@ $V_{Pin} = 4.3 V$	-	22	-	mA	Only applicable for QSPI0/1 data transmission
	QSPI0/1 signal pins (only when QSPI is enabled): QSPI0/1IO0 QSPI0/1IO1 QSPI0/1IO2 QSPI0/1IO3 SCK0/1 Output high current @ $V_{Pin} = 4.7 V$	-	10	-	mA	Only applicable for QSPI0/1 data transmission
I_{OH1}	General drive capability IO group outputting high current	-	12	-	mA	$V_{Pin} = 4.3 V$
		-	6	-	mA	$V_{Pin} = 4.7 V$
I_{lg1}	Input leakage current	-1	-	1	μA	IO is high-impedance input Mode $V_{IN} = V_{DD}$ or V_{SS}
R_{PH1}	Pull-up Resistor	15	30	45	$k\Omega$	$V_{IN} = V_{SS}$

27.5.2 $V_{DD} = 3.3 V$, $T_A = +25 ^\circ C$, unless otherwise specified

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
V_{IH3}	Input high voltage	$0.7 V_{DD}$	-	$V_{DD} + 0.3$	V	
V_{IL3}	Input low voltage	-0.3	-	$0.3 V_{DD}$	V	
V_{IH4}	Input high voltage	$0.8 V_{DD}$	-	V_{DD}	V	Schmitt Trigger Input: NRST
V_{IL4}	Input low voltage	-0.2	-	$0.2 V_{DD}$	V	T_CLK / T_DIO UART0 to 5 RXD Input SPI / TWI Signal Input INT0 to INT15

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
						PWM Fault Detection Input FLT Timer Clock Input Tn Timer Capture Input TnEX
I _{OL3}	Standard Drive Capability IO Group Output low current	-	20	-	mA	V _{Pin} = 0.4 V
		-	35	-	mA	V _{Pin} = 0.8 V
I _{OL4}	COM port IO group Output low current	-	40	-	mA	V _{Pin} = 0.4 V
		-	75	-	mA	V _{Pin} = 0.8 V
I _{OHQSPIB}	QSPI0/1 signal pins (Only when QSPI is Enabled): QSPI0/1IO0 QSPI0/1IO1 QSPI0/1IO2 QSPI0/1IO3 SCK0/1 Output high current @ V _{Pin} = 3.0 V	-	7	-	mA	Only applicable for data transmission
I _{OH2}	General drive capability IO group outputting high current	-	3.9	-	mA	V _{Pin} = 3.0 V
I _{lk2}	Input leakage current	-1	-	1	μA	IO is high-impedance input Mode V _{IN} = V _{DD} or V _{SS}
R _{PH2}	Pull-up Resistor	38	75	113	kΩ	V _{IN} = V _{SS}

27.6 TK electrical characteristics

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
I _{TK}	High Sensitivity Touch Key Operating Current @5 V	-	0.8	1.2	mA	f _{HCLK} = 32 MHz Clock Source: HIRC
	High-sensitivity touch key operating current @3.3 V	-	0.7	1.0	mA	f _{HCLK} = 32 MHz Clock Source: HIRC

27.7 BTM electrical characteristics

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
I _{BTM}	Base Timer Operating Current @5 V	-	1.2	-	μA	BTMCLKSEL = 0 BTM Clock Source is LIRC
	Base Timer Operating current @ 3.3 V	-	1.2	-	μA	BTMCLKSEL = 0 BTM Clock Source is LIRC

27.8 WDT electrical characteristics

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
I _{WDT}	WDT Working Current @5 V	-	1.2	-	μA	

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
	WDT working current @ 3.3 V	-	1.2	-	μA	

27.9 AC electrical characteristics

($V_{DD} = 2.0 \text{ V to } 5.5 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
T_{LXT}	Startup time of external 32.768k oscillator	-	1	-	s	External 32.768k crystal oscillator
T_{POR}	Power On Reset time	-	15	-	ms	
T_{PDW}	Power Down Mode Wake-up Time	-	65	130	μs	
T_{Reset}	Reset pulse width	18	-	-	μs	Active low
T_{LVR}	LVR debounce time	-	30	-	μs	
f_{HIRC}	HIRC oscillator stability	63.36	64	64.64	MHz	$V_{DD} = 2.0 \text{ to } 5.5 \text{ V}$ $T_A = -40 \text{ to } 105^\circ\text{C}$
f_{LIRC}	LIRC frequency	-	37	-	kHz	$V_{DD} = 2.0 \text{ to } 5.5 \text{ V}$ $T_A = -40 \text{ to } 105^\circ\text{C}$
	LIRC frequency drift	-4	-	4	%	$V_{DD} = 2.0 \text{ to } 5.5 \text{ V}$ $T_A = 25^\circ\text{C}$

27.10 ADC electrical characteristics

($T_A = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
V_{ADC}	Power Supply Voltage	2.4	5	5.5	V	$V_{ref} = 1.024 \text{ V}$
		2.7	5	5.5	V	$V_{ref} = 2.048 \text{ V}$
		2.7	5	5.5	V	$V_{ref} = 2.4 \text{ V}$
		2.0	5	5.5	V	$V_{ref} = V_{DD}$
V_{REF1}	Internal reference 2.048 V	2.028	2.048	2.068	V	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$ $T_A = 25^\circ\text{C}$
V_{REF2}	Internal reference 1.024 V	1.014	1.024	1.034	V	$V_{DD} = 2.4 \text{ to } 5.5 \text{ V}$ $T_A = 25^\circ\text{C}$
V_{REF3}	Internal reference 2.4 V	2.38	2.40	2.42	V	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$ $T_A = 25^\circ\text{C}$
V_{REF4}	Internal reference 2.048 V	2.007	2.048	2.089	V	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$ $T_A = -40 \text{ to } 105^\circ\text{C}$
V_{REF5}	Internal reference 1.024 V	1.004	1.024	1.044	V	$V_{DD} = 2.4 \text{ to } 5.5 \text{ V}$ $T_A = -40 \text{ to } 105^\circ\text{C}$
V_{REF6}	Internal reference 2.4 V	2.35	2.40	2.45	V	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$ $T_A = -40 \text{ to } 105^\circ\text{C}$
N_R	Precision / Resolution	-	14	-	bit	$GND \leq V_{AIN} \leq V_{DD}$
V_{AIN}	ADC input Voltage	GND	-	V_{DD}	V	

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
R_{AIN}	ADC input Resistance	1	-		$M\Omega$	$V_{IN} = 5\text{ V}$
I_{lk_ADC}	ADC input leakage current	-1	-	1	μA	$V_{IN} = V_{AINx}$
I_{ADC1}	ADC conversion current 1	-	1	2.2	mA	ADC module enabled $V_{DD} = 5\text{ V}$
I_{ADC2}	ADC conversion current 2	-	0.8	1.8	mA	ADC module enabled $V_{DD} = 3.3\text{ V}$
DNL	Differential nonlinearity error	-	± 6	-	LSB	$V_{DD} = 5\text{ V}$ $V_{REF} = 5\text{ V}$
INL	Integral nonlinearity error	-	± 8	-	LSB	
E_Z	Offset error	-	± 12	-	LSB	
E_F	Full scale error	-	± 14	-	LSB	
E_{AD}	Total absolute error	-	± 14	-	LSB	
T_{ADC}	ADC sampling + conversion total time	-	1.1	1.6	μs	$f_{HCLK} = 32\text{ MHz}$, Clock Source is HIRC LOWSP[2:0] = 100
		-	1.2	1.7	μs	$f_{HCLK} = 32\text{ MHz}$, Clock Source is HIRC LOWSP[2:0] = 101
		-	1.5	2.1	μs	$f_{HCLK} = 32\text{ MHz}$, Clock Source is HIRC LOWSP[2:0] = 110
		-	2.0	2.7	μs	$f_{HCLK} = 32\text{ MHz}$, Clock Source is HIRC LOWSP[2:0] = 111

27.11 CMP electrical characteristics

($V_{DD} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
V_{CM}	Input voltage range	0	-	V_{DD}	V	
V_{OS}	Offset voltage	-	10	30	mV	
V_{HYS}	Voltage Comparison Hysteresis	-	20	-	mV	
I_{CMP}	Comparator Conversion Current	-	-	100	μA	$V_{DD} = 5\text{ V}$
T_{CMP}	Response Time	-	-	2	μs	

27.12 OP electrical parameters

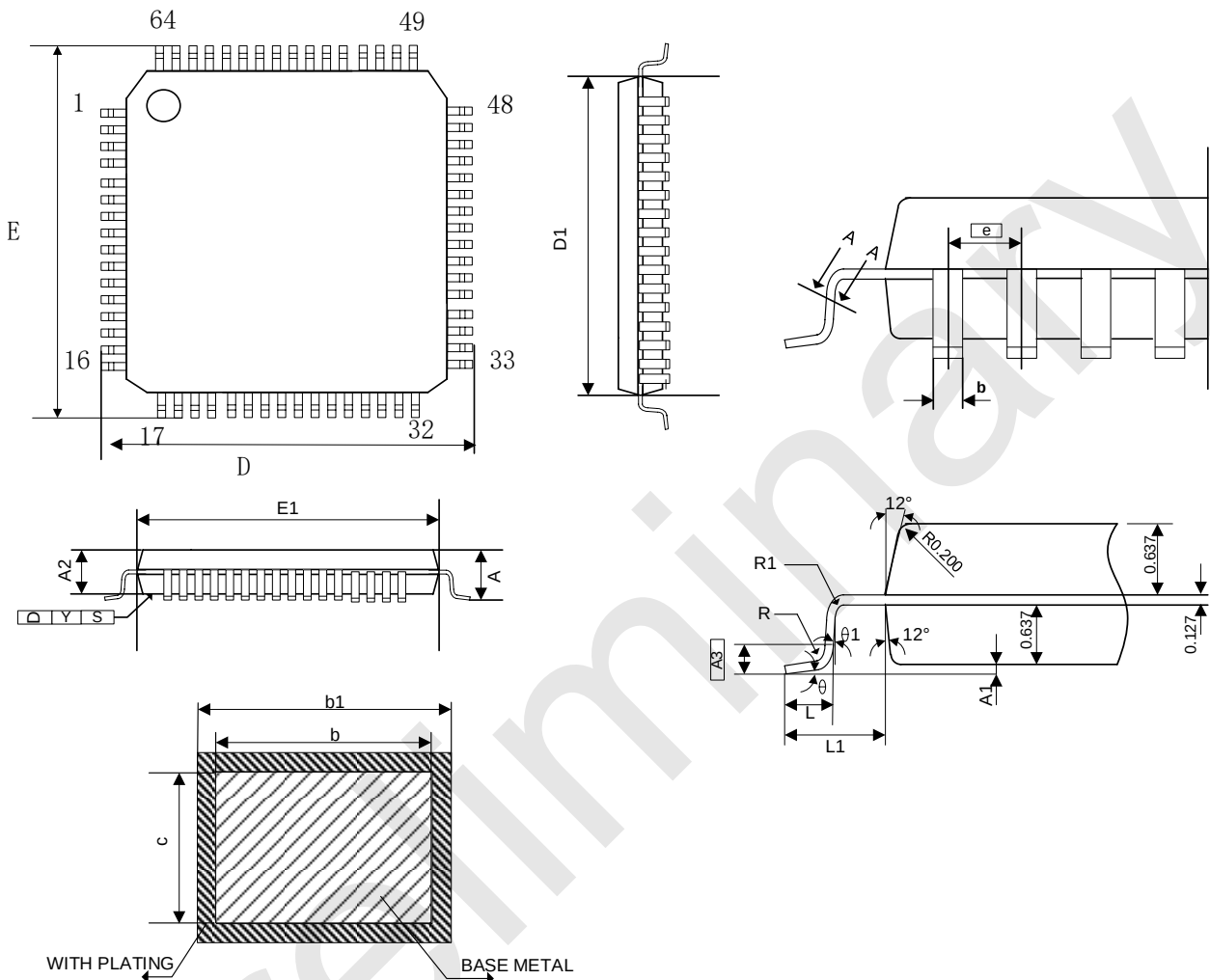
($V_{DD} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical values	Maximum Value	Unit	Condition
I _{OP}	PGA operating current	-	1	1.3	mA	
V _{OP}	OP operating voltage	2.8	-	5.5	V	
V _{OPO}	OP output voltage	0	-	V _{DD}	V	
V _{CMI}	Common-mode input voltage	0	-	V _{DD}	V	
V _{OFFSET}	Offset voltage	-1	-	1	mV	
I _{LOAD}	Load current	-	-	600	μA	
R _{LOAD}	Load resistor	8	-	-	kΩ	
C _{LOAD}	Load capacitor	-	-	30	pF	
CMRR	Common-mode rejection ratio	-	90	-	dB	
PSRR	Power supply rejection ratio	-	75	-	dB	
GBW	Gain-bandwidth product	-	40	-	MHz	
Slew rate	Slew rate	-	13	-	V/μs	
PM	Phase margin	-	60	-	°	CL = 50 pF
G _{PGA}	PGA non-inverting gain error	-5	-	5	%	Non-inverting gain = 8
		-5	-	5	%	Non-inverting gain = 16
		-5	-	5	%	Non-inverting gain = 32
		-5	-	5	%	Non-inverting gain = 64
	PGA Inverting Amplification Error	-5	-	5	%	Inverting gain = 7
		-5	-	5	%	Inverting gain = 15
		-5	-	5	%	Inverting gain = 31
		-5	-	5	%	Inverting gain = 63
R _{PGA}	PGA Non-inverting Amplification R2/R1 Resistance Ratio	-	70/10	-	kΩ/ kΩ	Non-inverting gain = 8
		-	150/10	-	kΩ/ kΩ	Non-inverting gain = 16
		-	310/10	-	kΩ/ kΩ	Non-inverting gain = 32
		-	630/10	-	kΩ/ kΩ	Non-inverting gain = 64
	PGA Inverting Amplification R2/R1 Resistance Ratio	-	70/10	-	kΩ/ kΩ	Inverting gain = 7
		-	150/10	-	kΩ/ kΩ	Inverting gain = 15
		-	310/10	-	kΩ/ kΩ	Inverting gain = 31
		-	630/10	-	kΩ/ kΩ	Inverting gain = 63
RΔ	Resistance Error of R1 or R2	-20	-	+20	%	

Note: Offset Voltage V_{OFFSET} and Phase Margin PM are guaranteed by design.

28 Package information

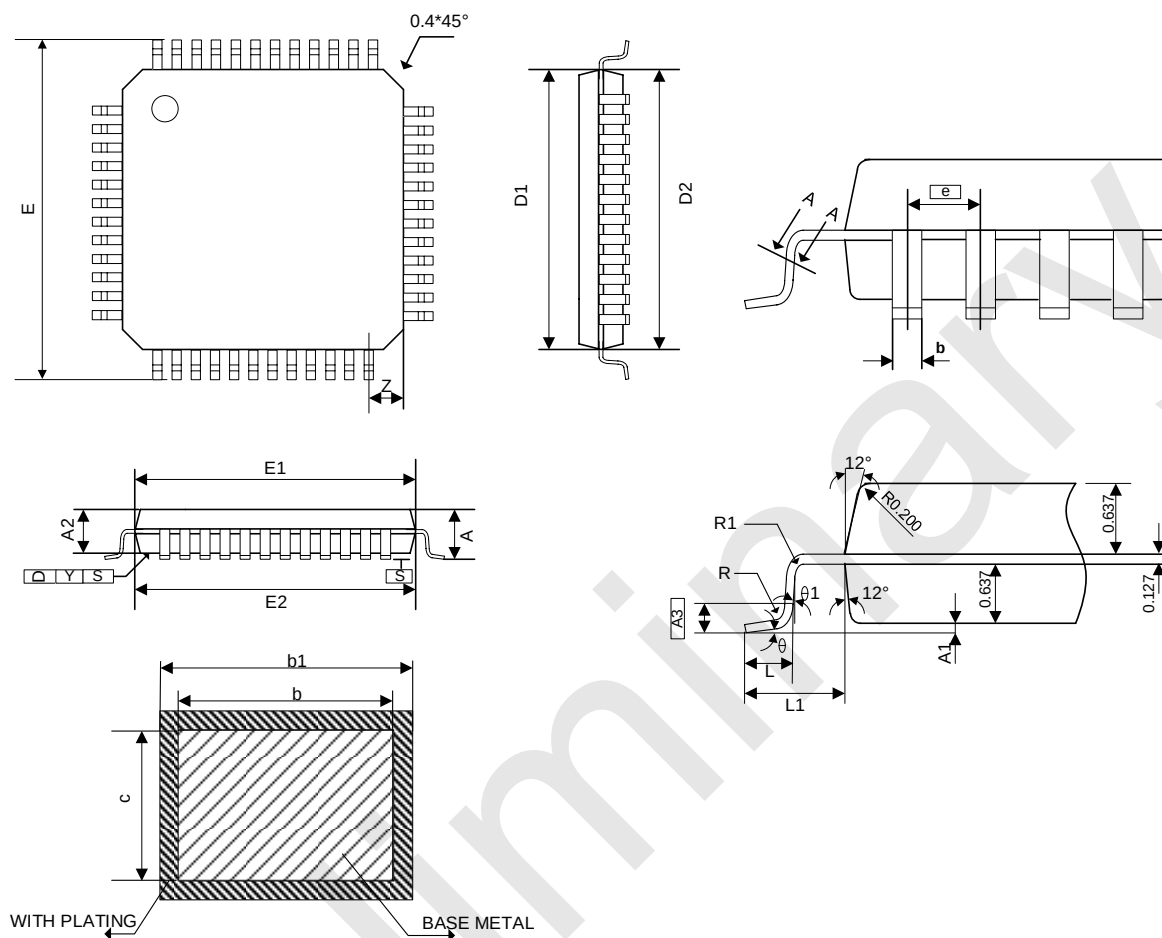
LQFP64 (10X10) Package Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	1.40	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	-	0.23
b1	0.17	-	0.26
c	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	-	0.50 BSC	-
L	0.45	-	0.75

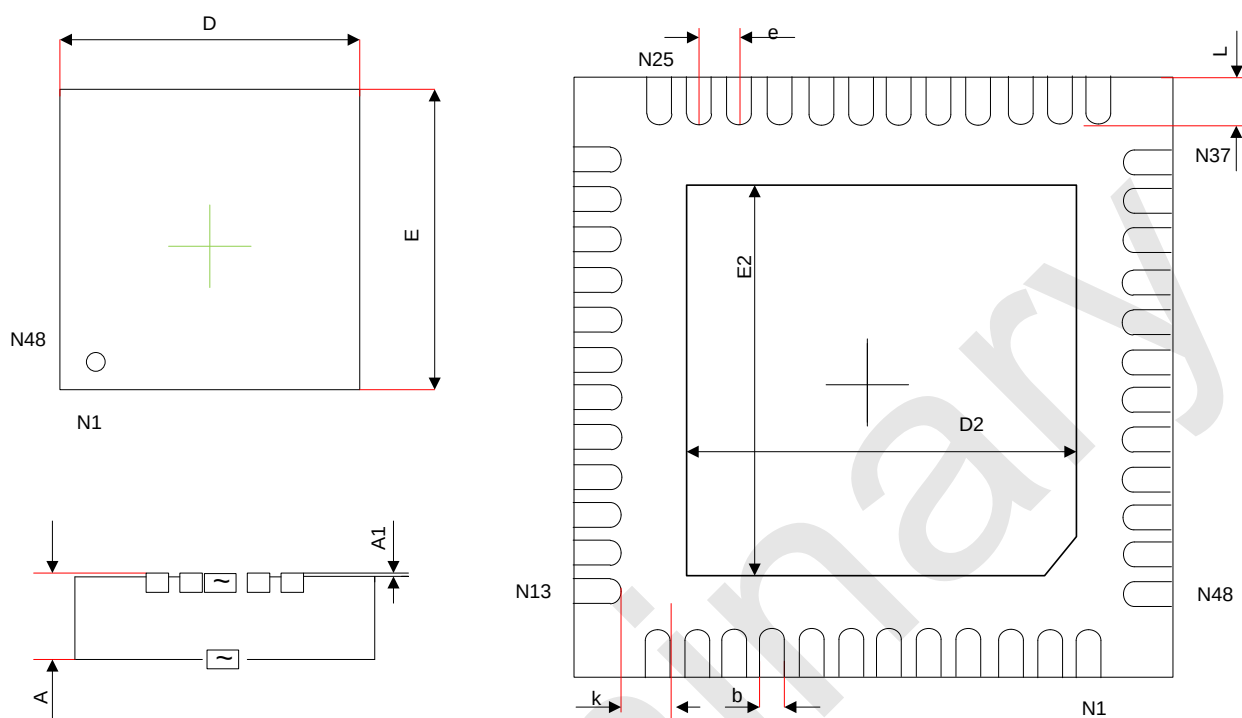
Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
L1	-	1.00REF	-
R	0.08	-	-
R1	0.08	-	0.20
θ	0°	3.5°	7°

LQFP48 (7X7) Package Dimensions (Unit: mm)



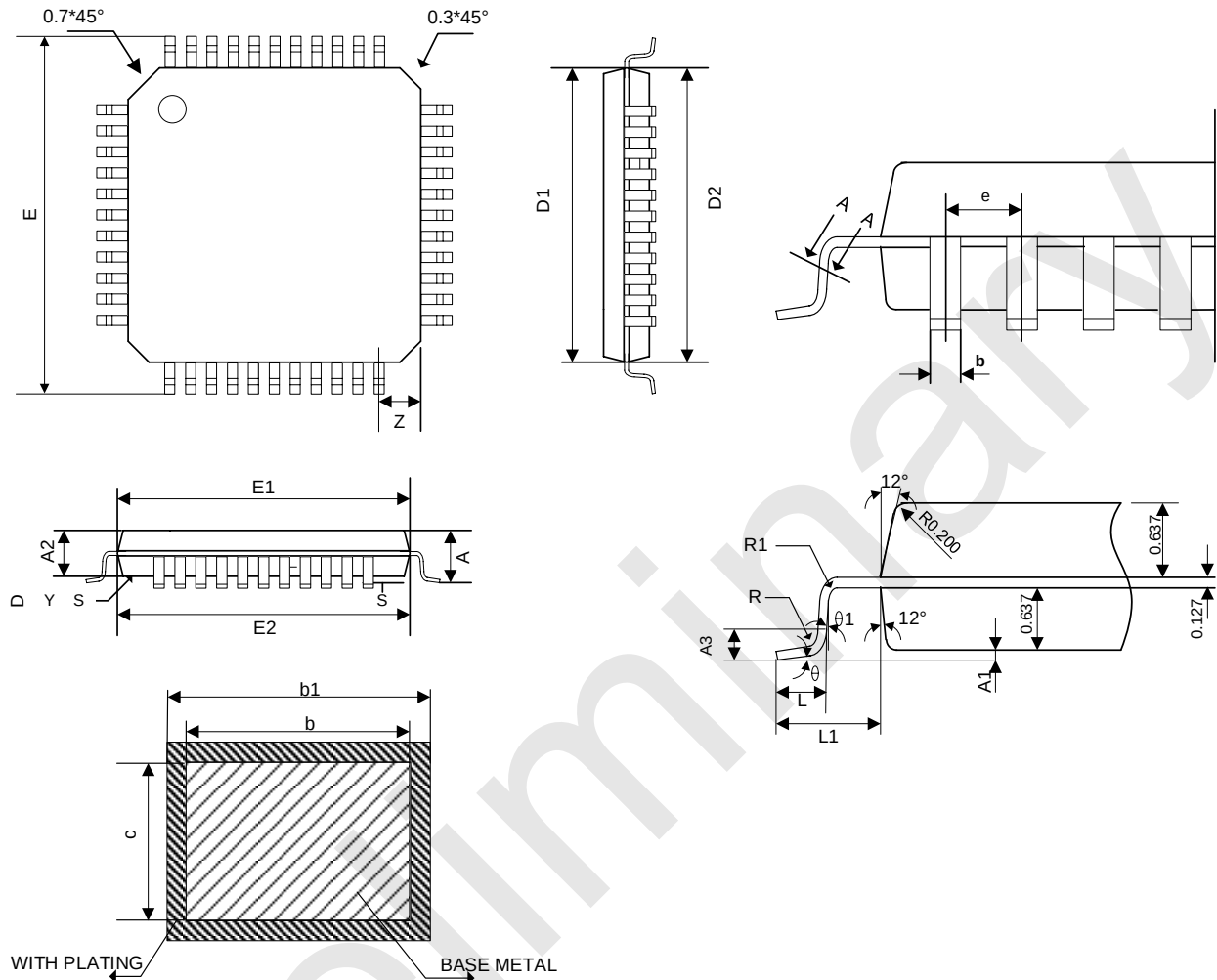
Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.15	0.20	0.25
b1	0.16	0.22	0.28
c	0.12	--	0.17
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	--	0.5	--
L	0.43	--	0.75
L1	0.90	1.0	1.10

Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
$\theta 1$	0°	--	--
y	--	--	0.1
Z	--	0.75	--

QFN48 (5X5) Package Dimensions (Unit: mm)


Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.12	--	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35 BSC.		
k	0.20	0.30	--
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40

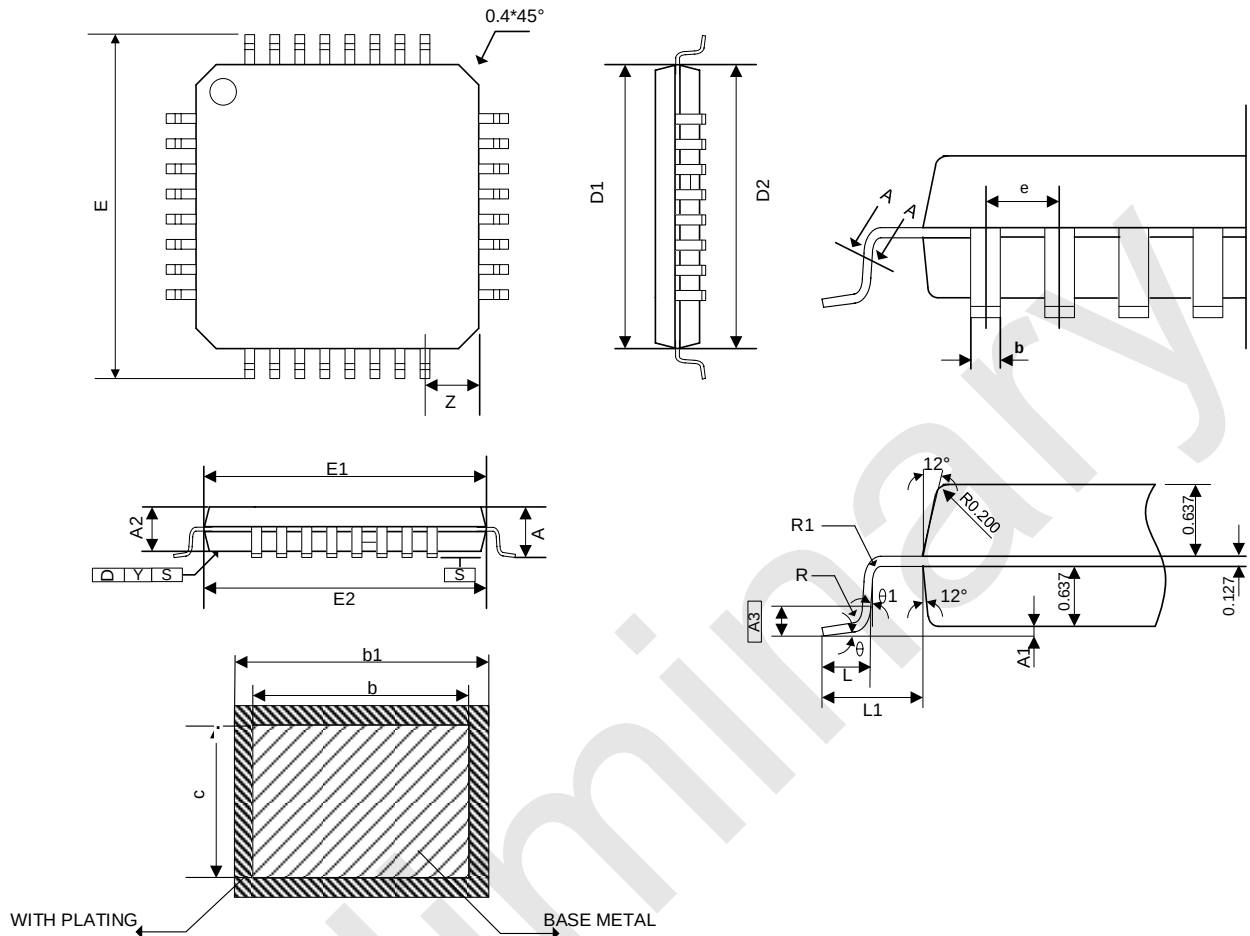
LQFP44 (10X10) Package Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	1.45	1.55	1.65
A1	0.015	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.25	0.30	0.36
b1	0.26	0.32	0.38
c	0.12	0.13	0.14
D1	9.85	9.95	10.05
D2	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.85	9.95	10.05
E2	9.90	10.00	10.10
e	--	0.8	--
L	0.42	--	0.75

Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
L1	0.95	1.0	1.15
R	0.08	--	0.25
R1	0.08	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	1.0	--

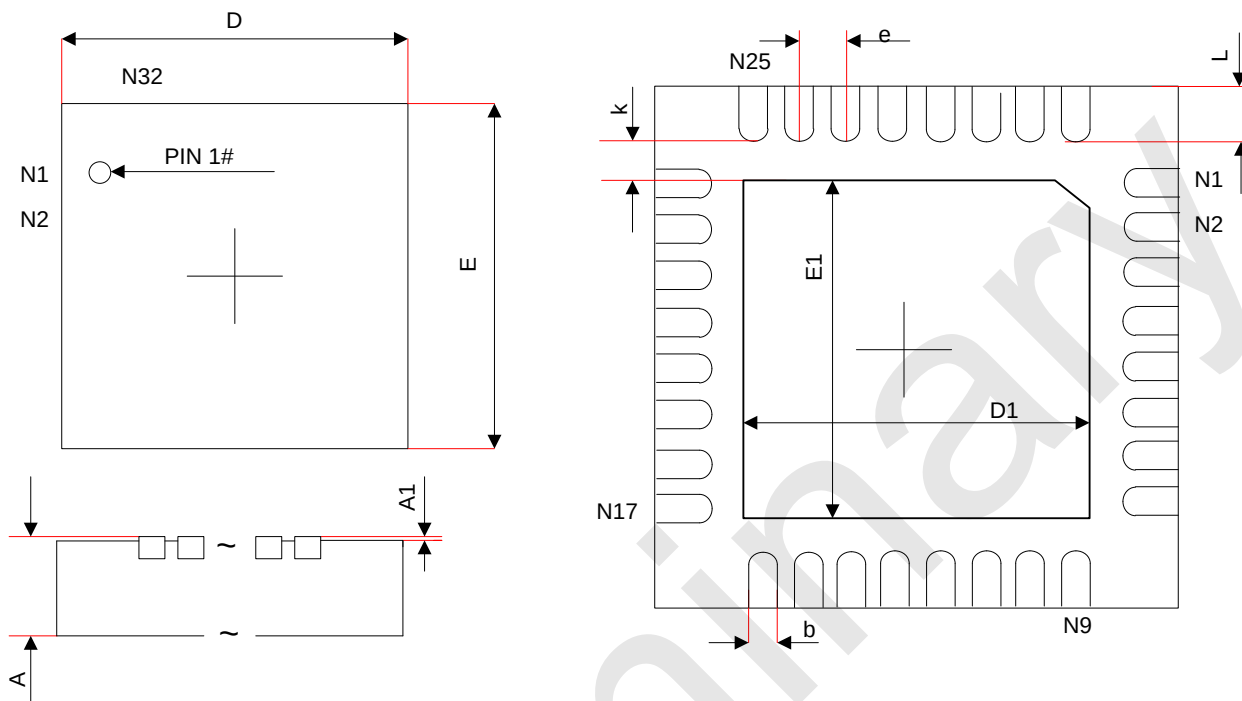
LQFP32 (7X7) Package Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.30	1.40	1.50
A3	--	0.254	--
b	0.30	0.35	0.41
b1	0.31	0.37	0.43
c	0.12	0.13	0.14
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	--	0.8	--
L	0.43	--	0.75
L1	0.90	1.00	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°

Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
θ_1	0°	--	--
y	--	--	0.1
Z	--	0.70	--

QFN32 (4X4) Package Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40 BSC		
k	0.20	-	-
D1	2.60	--	2.90
E1	2.60	--	2.90
L	0.22	--	0.45

29 Revision history

Version	Record	Date
V0.1	First Edition	June 26, 2026

Preliminary

30 Important notice

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Preliminary