1 General Description

The SC32F12T/12G is a series of industrial-grade Flash microcontrollers based on the Arm Cortex®-M0+ core, featuring touch functionality. These microcontrollers operate at a high frequency of up to 64MHz. The Cortex®-M0+ core utilizes a 32-bit reduced instruction set architecture (RISC) and complies with the CMSIS standard. The SC32F12T/12G series offers powerful data processing capabilities, with an integrated Direct Memory Access (DMA) controller for high-speed data transfer. The hardware CRC module and the built-in 32-bit hardware multiplier further enhance the data computation speed.

The SC32F12T/12G microcontrollers incorporate two clock sources: a high-precision high-frequency 64MHz oscillator (HIRC), a low-frequency 32kHz oscillator (LIRC). Additionally, they provide two external crystal oscillator interfaces: a 2-16MHz high-frequency crystal (HXT) interface and a 32.768 KHz low-frequency crystal (LXT) interface, HXT ports are multiplexed with LXT ports. The embedded clock sources and external crystal oscillator interfaces can supply the system clock, and the built-in system clock monitor module switches to HIRC as the clock source in case of system clock abnormalities.

The SC32F12T/12G series offers a wide range of peripheral resources, including a built-in 39-channel high-sensitivity capacitive touch circuit, up to 46 GPIO pins with external interrupt support, 8 16-bit timers, 8 channels of up to 64MHz 16-bit multifunctional PWM with fault detection function, and 32 channels of 8-bit LEDPWM. It also features 6 independent UARTs, among which UART2 features a complete LIN interface and support both master and slave modes. 3 independent SPIs, 2 independent TWIs, built-in LCD/LED hardware drivers, 1 analog comparator, 1 rail-to-rail OP, and 18 channels of 14-bit high-precision ADC. The microcontrollers come with an independent watchdog timer (WDT) and a low-voltage reset circuit (LVR) to enhance system reliability. They provide three power modes to meet various power consumption requirements in different application scenarios.

The SC32F12T/12G series delivers high performance and reliability, supporting a wide operating voltage range of 2.0-5.5V and capable of operating in an ambient temperature range of -40°C to 105°C. They also exhibit excellent ESD performance and EFT immunity. In terms of process technology, the SC32F12T/12G series adopts the industry-leading eFlash process, allowing for more than 100,000 write cycles and data retention of 100 years at room temperature. Regarding storage resources, the SC32F12T/12G series offers a maximum of 512 Kbytes of ROM space and 16 Kbytes of SRAM The SRAM also supports parity check functionality for data integrity. Additionally, there is a 1.5 Kbytes user storage area(generic EEPROM), and a 4 Kbytes system storage area(LDROM). It includes a built-in system storage area to support OTA upgrades and provides multiple programming methods such as ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application Programming), enabling on-board debugging and firmware updates while the chip is online or powered.

The SC32F12T/12G series excels in touch key (TK) characteristics and possesses outstanding anti-interference performance. It can be adapted to various touch button and master control solutions, finding applications in a wide range of industries including smart appliances, smart homes, the Internet of Things (IoT), wireless communications, gaming consoles, industrial control, and consumer electronics.

2 Features

Operating Conditions

- Operating voltage: 2.0V~5.5V
- Operating temperature: -40 ~ +105℃

EMS

- ESD
  - HBM：JEDECEIA/JESD22-A114F Class 3A
  - MM：JEDEC EIA/JESD22-A115C Class C
  - CDM：ANSI/ESDA/JEDEC JS-002-2022 Class C3

Package

- 48 PIN: LQFP48 (7X7) / QFN48 (5X5)
- 44 PIN: LQFP44 (10X10)
- 32 PIN: LQFP32 (7X7) / QFN32 (4X4)
- 28 PIN: SOP28 / TSSOP28

Core

- Cortex®-M0+ core
- With Wakeup Interrupt Controller (WIC) module
- With MPU module
- 64-bits instruction prefetch
- Built-in Multiplier Unit (MDU)

Reset

- Power-On Reset (POR)
- Software Reset
- Reset through external NRST pin (PC8) with a low-level signal
- Watchdog Timer (WDT) reset
- Low Voltage Reset (LVR)
  - Four selectable reset voltages: 4.3V, 3.7V, 2.9V, 1.9V
  - The default value is determined by the user's programmed Code Option

BUS

- 1 IOPORT
- 1 AHB
- 3 APB：APB0~APB2

Power Saving Mode

- Low-Speed Mode, system clock source can be selected as LIRC, and CPU can work at 32MHz
- IDLE Mode, can be woken up by any interrupt
- STOP Mode, can be woken up by INT0~15, Base Timer, TK, and CMP

2.1 Flash

APROM

- Up to 512 Kbytes APROM
- Can be rewritten up to 100,000 times
- Supports hardware read protection encryption
- Supports hardware write protection: Provides two regions for disabling IAP (In-Application Programming) operations. Users can configure the settings through the Code Option, with the minimum setting unit being 512 bytes (one sector)

LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program

SRAM

- 16 Kbytes Internal SRAM
- Supports parity check:
  - An additional 2K RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte).
  - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
  - Provides an independent SRAM parity error flag, SRAMPEIF.
  - Pay attention to the initialization of the SRAM when in use.
- Supports booting from SRAM

1.5K Bytes User Storage Aera(generic EEPROM)

- Divided into three 512 bytes sectors
- Can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature

96 bits unique ID

- 96-bit Unique ID defined in the design option area

2.2 BootLoader

- Hardware method: System storage area of 4 Kbytes, factory-programmed with BootLoader program
- Software method: Supports interrupt vector table remapping, allowing flexible partitioning of the APROM area for user BootLoader program execution

2.3 Flash Programming and Emulation

- Programming methods supported: ICP / ISP / IAP
- 2-wire JTAG / SWD programming and emulation interface
- Simulation functionality is not supported in encrypted mode

2.4 Clock source

Built-in high-frequency 64 MHz oscillator (HIRC)

- Can be selected as the system clock source
- The default clock frequency when power on "f_{SYS}" is $f_{HIRC}/2$
- Frequency Error: Within ±1% @ -40 ~ 105℃ @ 2.0V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

Built-in low-frequency 32 kHz oscillator (LIRC)

- Can be selected as the system clock source
- Fixed as the WDT clock source, which will be automaticlly enabled when WDT is enabled
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Frequency Error: Within ±4% @ -20 ~ 85℃ @ 4.0V~ 5.5V, after register correction

External 2~16MHz crystal oscillator (HXT)

- Can be selected as the system clock source
- User can choose an external crystal oscillator oscillating frequency of <12MHz or ≥12MHz

External 32.768 KHz crystal oscillator (LXT)

- Can be selected as the system clock source

- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Allows for an external 32.768kHz oscillator
- Automatic calibration of HIRC can be performed using LXT

2.5 Interrupts (INT)

- Up to 25 interrupts
- Four-level interrupt priority can be set
- External interrupts (INT):
  - 16 interrupts, occupying 4 interrupt vectors in total
  - Change Interrupts on All GPIO pins
  - All interrupts can be set as rising edge, falling edge, or both-edge interrupts, each with an independent corresponding interrupt flag
  - Setting the corresponding interrupt flag in software triggers entry into the corresponding interrupt

2.6 Digtal peripherals

Up to 46 GPIOs

- Independent pull-up resistor configuration is available
- All GPIO pins have source driving capability controlled by four levels
- All GPIO pins have high sink current driving capability (50mA)

Watchdog timer (WDT)

- Built-in WDT with programmable overflow time ranging from 3.94ms to 500ms

Base Timer（BTM）

- The clock sources LXT and LIRC are selectable
- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

8 16-bit timers: Timer0~Timer7

- 16-bit up, down, and up/down auto-reload counters
- Supports rising edge/falling edge capture for PWM duty and period capture
- Each TIM can provide two channels of synchronized and adjustable duty cycle PWM outputs (TPWMA/TPWMB).
- TIM1/2/6 timer overflow and capture events can trigger DMA requests

8 channels 16-bit Advanced PWM0

- The clock source can be selected up to 64MHz
- Shared period and independently adjustable duty cycle
- Support dead time and complementary PWM output
- Support center-aligned mode
- Support fault detection

32 channels 8-bit LEDPWM

- Shared period and independently adjustable duty cycle
- Support center-aligned mode

6 independent UART: UART0~5

- UART2 has a full LIN interface, offering the following capabilities:
  - Master and slave mode switching
  - Hardware break transmission in master mode(10/13bits)
  - Hardware break detection in slave mode(10/11bits)
  - Baud rate synchronization in slave mode
  - Provision of related interrupts, status bits, and flags
- Each UART ports can be mapped to 2 sets of IO pins
- Independent baud rate generator
- UART2 does not support wake-up from STOP Mode
- UART0/1/3/4/5 support wake-up from STOP Mode
- Three communication modes available
  - Mode 0: 8-bit half-duplex synchronous communication
  - Mode 1: 10-bit full-duplex asynchronous communication
  - Mode 3: 11-bit full-duplex asynchronous communication
- UART0 and UART1 support DMA requests
- UART2~5 do not support DMA requests

3 independent SPI: SPI0~2

- SPI0:
  - A 16-bit 8-level FIFO with separate transmit and receive
  - In SPI mode, the drive capability of the corresponding signal pins will be enhanced
  - Can be mapped to 4 sets of ports
  - Supports DMA
- SPI1:
  - Can be mapped to 4 set of ports
  - Supports DMA
- SPI2:
  - Can be mapped to 4 set of ports
  - Do not support DMA

2 independent TWI: TWI0/TWI1

- Supports master mode or slave mode
- Supports clock stretching in slave mode
- Communication speed of up to 1Mbps
- TWI0 supports DMA
- TWI0 signal ports can be mapped to 6 set of ports
- TWI1 signal ports can be mapped to 6 set of ports

CRC

- Initial value can be set, with a default of 0xFFFF_FFFF
- Polynomial can be programmed, with a default of 0x04C1_1DB7
- Supports 8/16/32-bit data units

LCD/LED Driver

- The clock sources LXT and LIRC are selectable
- LCD and LED are mutually exclusive options, sharing registers and ports
- LED:
  - Supports 8 X 24, 6 X 26, 5 X 27, or 4 X 28 segment LED driving
  - LED segment port has source driving capability controlled by four levels
  - Shares registers with 32-channel LEDPWM, allowing LED replacement driving and grayscale adjustment through center-aligned PWM waveforms
- LCD:
  - Supports 8 X 24, 6 X 26, 5 X 27, or 4 X 28 segment LCD driving
  - LCD voltage output port has selectable voltage divider resistor values
  - Two bias voltages options: 1/3 and 1/4
  - Two waveform modes: Type A and Type B
  - Three frame frequencies available:
    - 32/64/128 Hz in Type A mode
    - 64/128/256 Hz in Type B mode

DMA

- 2 independent configurable channels
- Each DMA channel can send DMA requests to other channels
- Data width supports byte, half-word, and word
- 22 DMA request sources with four priority levels
- Supports source/destination address auto-increment or fixed
- Supports single and burst transfer modes
- Transfer modes: memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral

2.7 Analog peripherals

39-channel high-sensitivity Touch Key circuit

- Exclusive to the SC32F12T series
- Channels can be scanned in parallel
- CMOD capacitor can only be externally connected
- Supports self-capacitance mode and mutual-capacitance mode
- Supports low-power mode
- Supports fast wake-up STOP mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

Analog-to-Digital Converter ADC

- Precison: 14 bits
- Supports up to 18 channels
  - External 16 ADC sampling channels can be multiplexed with I/O ports for other functions
  - One internal ADC can directly measure VDD voltage
  - One internal ADC can directly measure OP output
- Four options for ADC reference voltage: VDD, and internal 2.048V, 1.024V, or 2.4V
- Configurable ADC conversion completion interrupt
- Supports single-channel continuous conversion mode
- Supports DMA transmission: DMA request will be generated after ADC conversion complete
- The conversion results feature an overflow flag: OVERRUN, and the OVERRUN flag bit is located in the same register as the ADC conversion results so users can read the information all at once.

Operational Amplifier(OP)

- A rail-to-rail input stage
- Can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 8/16/32/64
  - Inverting gain: 7/15/31/63
- Two external pins for the non-inverting input: OP_P0 or OP_P1
- One external pin for the inverting input: OP_N
- One external pin for the output: OP_O
- The output can be directly connected to the ADC input
- The output can be directly connected to the positive input of a Comparator (CMP)

Analog Comparator CMP

- Five positive input signal selectable:
  - Four analog signal positive input terminals: CMP0~CMP3
  - OP output signal
- Negative input voltage can be selected from CMPR input or one of the 15 comparison voltages derived from the internal VDD voltage division
- CMP interrupts can wake up the STOP mode

Product Peripheral Resourse Table

Model Peripherals	SC32F12T_ SC32F12G_															
	_C9	_S9	_K9	_G9	_C8	_S8	_K8	_G8	_C7	_S7	_K7	_G7	_C6	_S6	_K6	_G6
GPIOs	46	42	30	26	46	42	30	26	46	42	30	26	46	42	30	26
APROM (Kbyte)	512				256				128				64			
SRAM (Kbyte)	16															
TK	SC32F12T_(with TK) & SC32F12G_(without TK)															
SPI	3															
TWI	2															
UART	6															
TIM	8	7	4	4	8	7	4	4	8	7	4	4	8	7	4	4
PWM0	8	8	8	4	8	8	8	4	8	8	8	4	8	8	8	4
LEDPWM	32	32	20	20	32	32	20	20	32	32	20	20	32	32	20	20
ADC Channels	16	16	8	8	16	16	8	8	16	16	8	8	16	16	8	8
LCD/LED segment	28	28	20	20	28	28	20	20	28	28	20	20	28	28	20	20
LCD/LED com	8	8	4	4	8	8	4	4	8	8	4	4	8	8	4	4
CRC	YES															
DMA	YES															
Max. CPU frequency	64MHz															

Products naming rules

SC	32	F	1	2	T	C	9	P	J	R

Campany Name
SinOne

Device family
8=8bit
32=32bit

Device type
A=Automotive
F/G=General
L=Ultra-low power
H=High performance
W=Wireless

CPU core
0= Cortex-M0
1= Cortex-M0+

Subseries1
0~9

Subseries2
T=TK
G=GP
M=Motor

Pin count

Label	D	F	E	G	K	T	H	S	C	U	R	J	M	O
Pin count	14	20	24	28	32	36	40	44	48	63	64	72	80	90
Label	V	Q	Z	A	I	B	N	X						
Pin count	100	132	144	169	176	208	216	256						

Flash memory size

Label	0	1	2	3	4	5	6	7	8	9	A	B	C	D
Size（KB）	1	2	4	8	16	32	64	128	256	512	1024	2048	-	-
Label	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Size（KB）	-	-	-	-	-	-	-	72	96	192	384	768	1536	-

Package type

Label	D	M	X	F	T	P	Q	K	S	Y	H	U	W
Package	DIP	SOP	TSSOP	QFP	TQFP	LQFP	QFN	SKDIP	MSOP	WLCSP	BGA	SOT	Wafer

Temperature range
I= -40°C~85°C Industrial
J= -40°C~105°C Automotive G2
A= -40°C~125°C Automotive G1
T= -40°C~150°C Automotive G0

Pack type

R	Tray
T	Tape and Reel
U	Tube
B	Bulk

Ordering Information

PRODUCT ID	PACKAGE	PACK
SC32F12TC9PJR	LQFP48	TRAY
SC32F12TC8PJR	LQFP48	TRAY
SC32F12TC7PJR	LQFP48	TRAY
SC32F12TC6PJR	LQFP48	TRAY
SC32F12GC9PJR	LQFP48	TRAY
SC32F12GC8PJR	LQFP48	TRAY
SC32F12GC7PJR	LQFP48	TRAY
SC32F12GC6PJR	LQFP48	TRAY
SC32F12TC9QJR	QFN48	TRAY
SC32F12TC8QJR	QFN48	TRAY
SC32F12TC7QJR	QFN48	TRAY
SC32F12TC6QJR	QFN48	TRAY
SC32F12GC9QJR	QFN48	TRAY
SC32F12GC8QJR	QFN48	TRAY
SC32F12GC7QJR	QFN48	TRAY
SC32F12GC6QJR	QFN48	TRAY
SC32F12TS9PJR	LQFP44	TRAY
SC32F12TS8PJR	LQFP44	TRAY
SC32F12TS7PJR	LQFP44	TRAY
SC32F12TS6PJR	LQFP44	TRAY
SC32F12GS9PJR	LQFP44	TRAY
SC32F12GS8PJR	LQFP44	TRAY
SC32F12GS7PJR	LQFP44	TRAY
SC32F12GS6PJR	LQFP44	TRAY
SC32F12TK9PJR	LQFP32	TRAY
SC32F12TK8PJR	LQFP32	TRAY
SC32F12TK7PJR	LQFP32	TRAY
SC32F12TK6PJR	LQFP32	TRAY
SC32F12GK9PJR	LQFP32	TRAY
SC32F12GK8PJR	LQFP32	TRAY
SC32F12GK7PJR	LQFP32	TRAY
SC32F12GK6PJR	LQFP32	TRAY
SC32F12TK9QJR	QFN32	TRAY

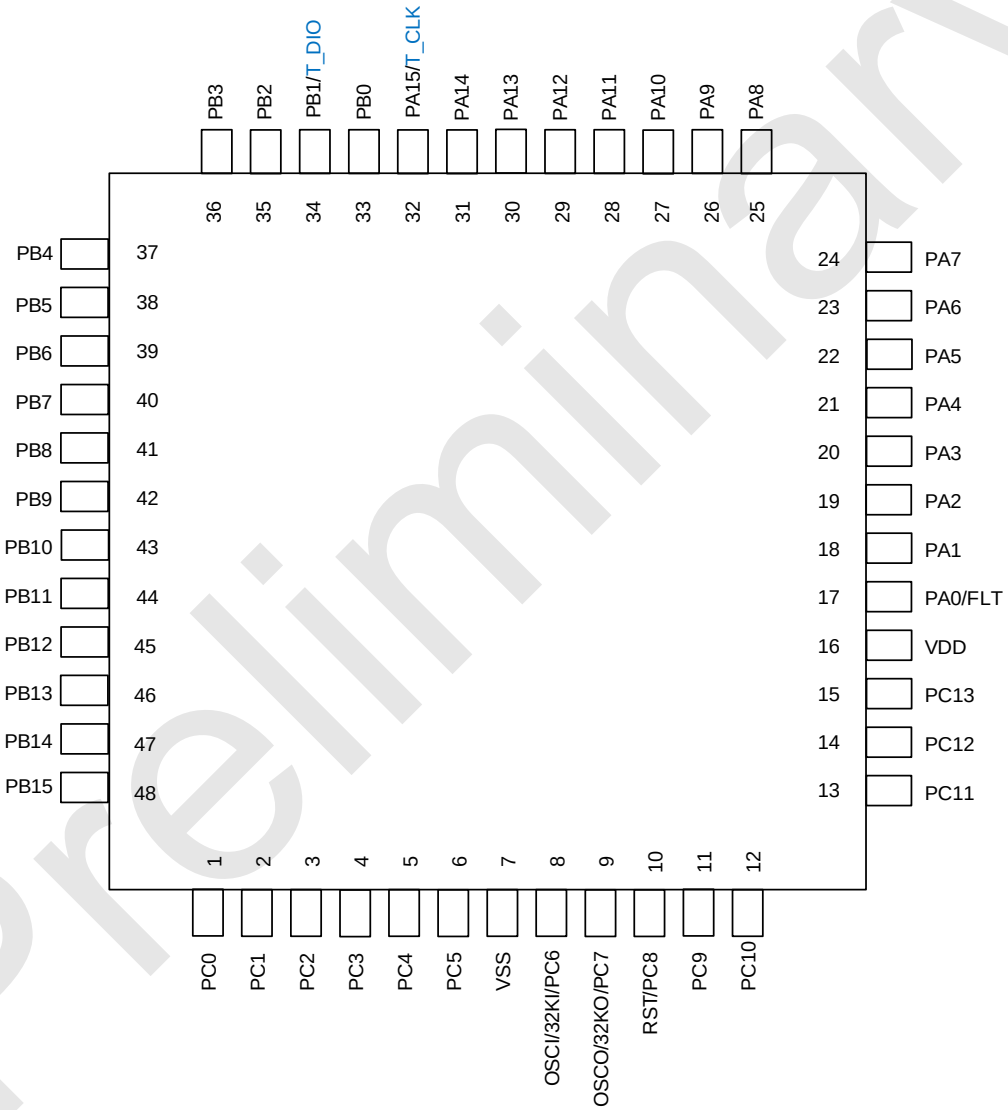
PRODUCT ID	PACKAGE	PACK
SC32F12TK8QJR	QFN32	TRAY
SC32F12TK7QJR	QFN32	TRAY
SC32F12TK6QJR	QFN32	TRAY
SC32F12GK9QJR	QFN32	TRAY
SC32F12GK8QJR	QFN32	TRAY
SC32F12GK7QJR	QFN32	TRAY
SC32F12GK6QJR	QFN32	TRAY
SC32F12TG9MJU	SOP28	TUBE
SC32F12TG8MJU	SOP28	TUBE
SC32F12TG7MJU	SOP28	TUBE
SC32F12TG6MJU	SOP28	TUBE
SC32F12GG9MJU	SOP28	TUBE
SC32F12GG8MJU	SOP28	TUBE
SC32F12GG7MJU	SOP28	TUBE
SC32F12GG6MJU	SOP28	TUBE
SC32F12TG9XJU	TSSOP28	TUBE
SC32F12TG8XJU	TSSOP28	TUBE
SC32F12TG7XJU	TSSOP28	TUBE
SC32F12TG6XJU	TSSOP28	TUBE
SC32F12GG9XJU	TSSOP28	TUBE
SC32F12GG8XJU	TSSOP28	TUBE
SC32F12GG7XJU	TSSOP28	TUBE
SC32F12GG6XJU	TSSOP28	TUBE

Content

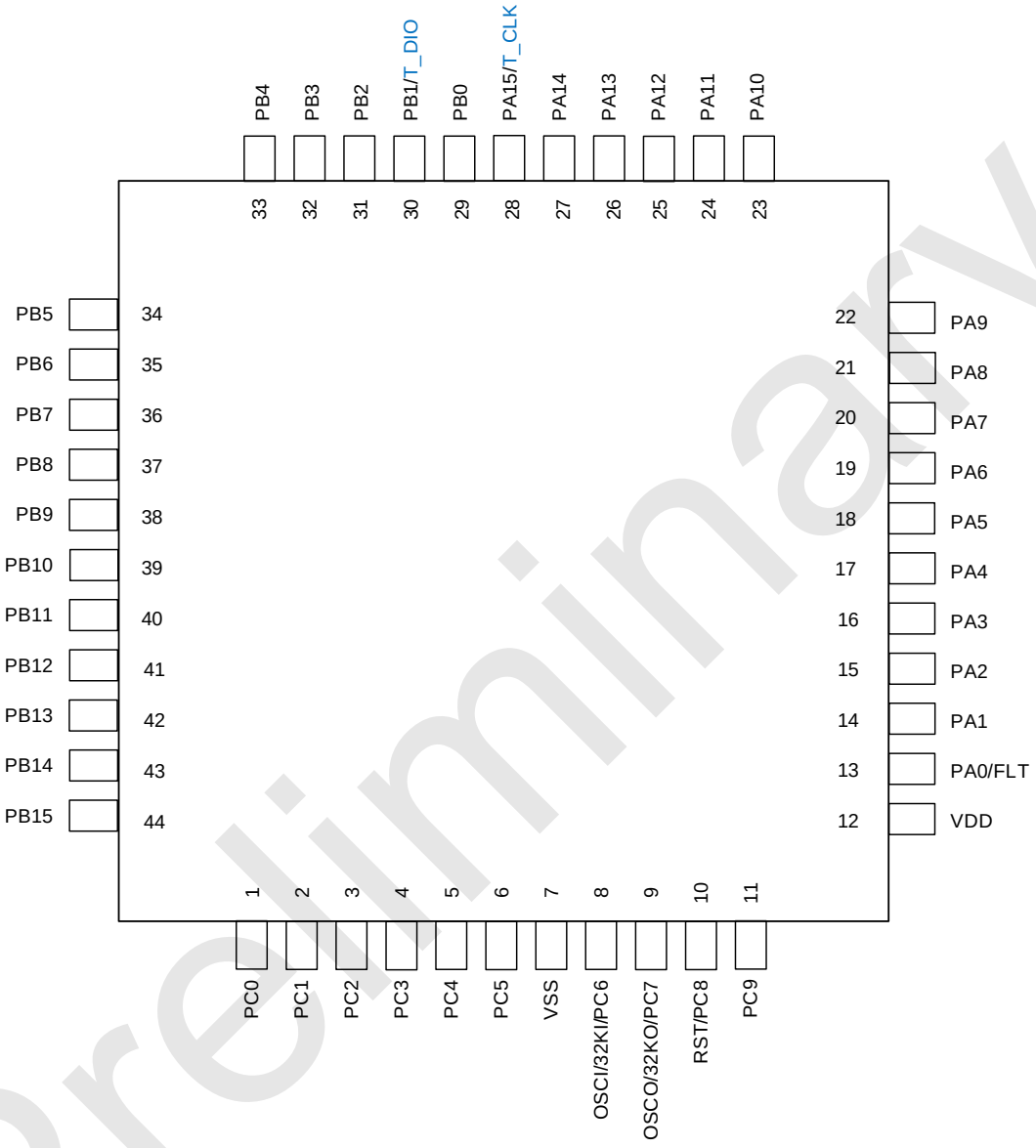
3 Pin Description

3.1 Pin Configuration

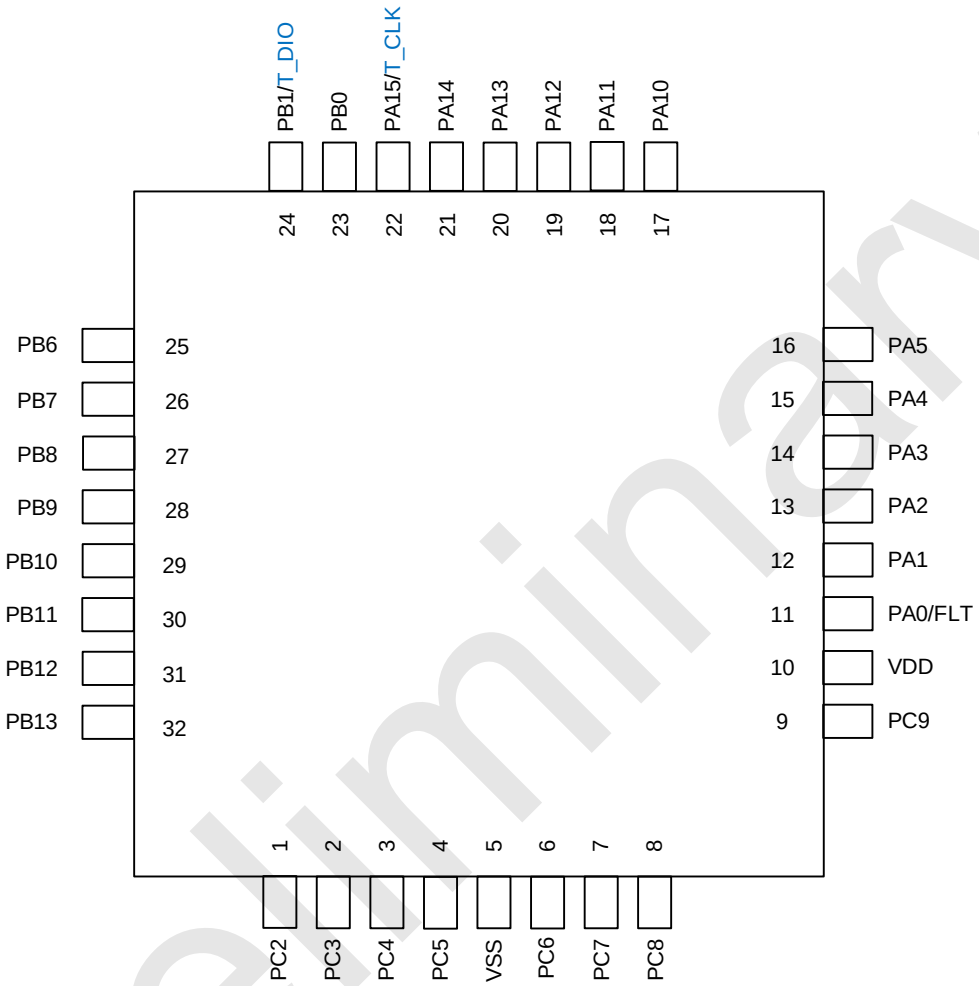
Note： TK function is supported exclusively by the SC32F12T series. In consideration of multiplexing of TK9/TK11 and TK debugging communication ports of the SC32F12T, if it is required to use the TK debugging function, please avoid using TK9TK11!



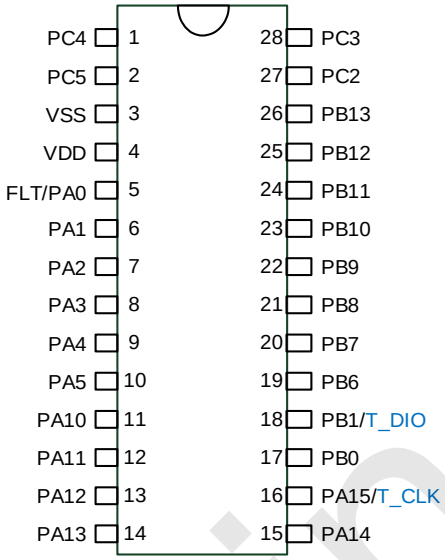
48PIN Pin Diagram
Suitable for LQFP48 & QFN48 package



44PIN Pin Diagram
Suitable for LQFP44 package



32PIN Pin Diagram
Suitable for LQFP32 & QFN32 package



28PIN Pin Diagram
Suitable for SOP28 & TSSOP28 package

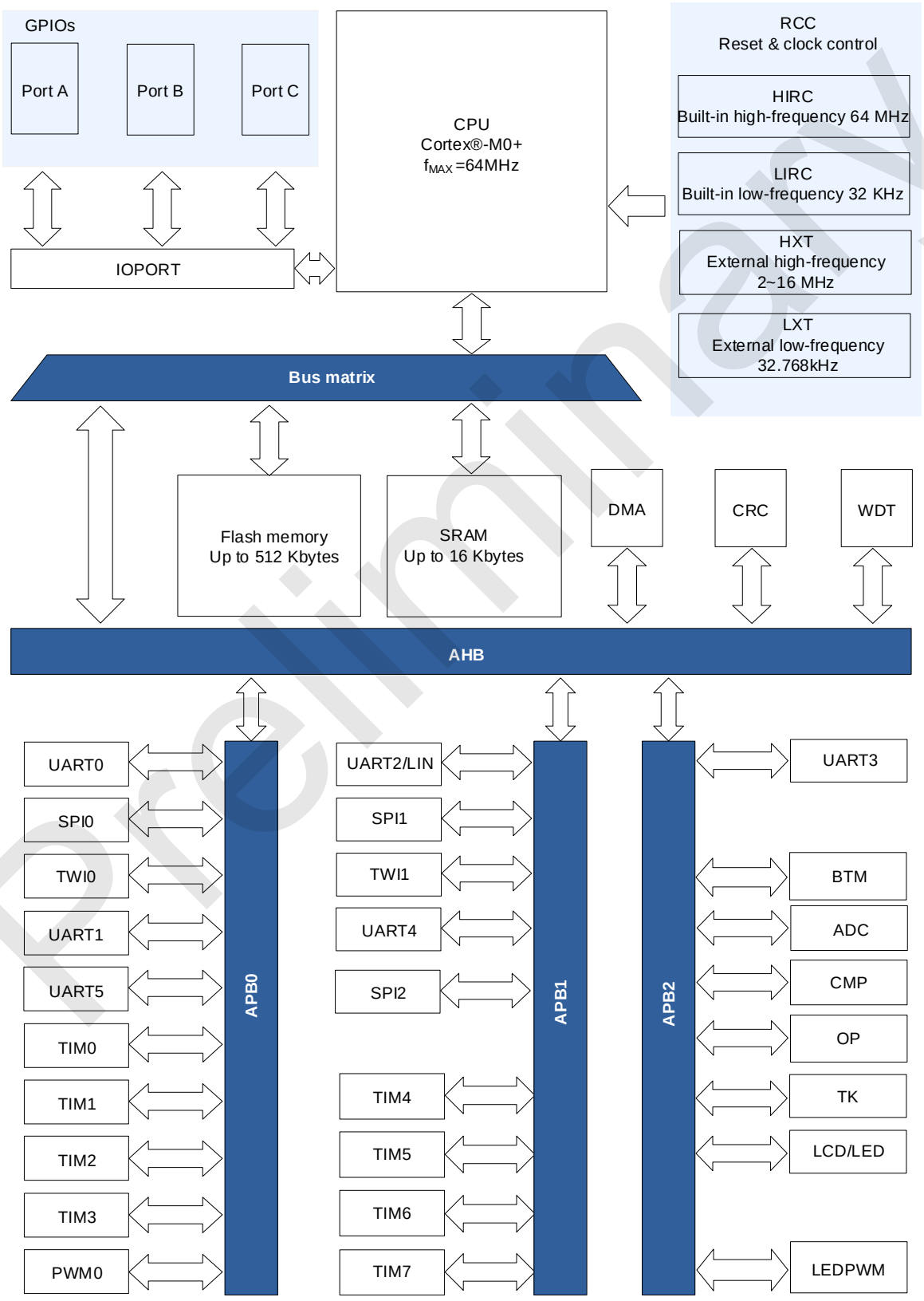
3.2 Pin Resource List

Note: TK function is supported exclusively by the SC32F12T series. In consideration of multiplexing of TK9/TK11 and TK debugging communication ports of the SC32F12T, if it is required to use the TK debugging function, please avoid using TK9TK11!

LQFP48/QFN48	LQFP44	LQFP32/QFN32	SOP28/TSSOP28	Pin Name	Special	TK	LCD/LED	OP	ADC	CMP	LEDPWM	PWM0	UART	SPI	TWI	TnPWM	TnEX/Tn	INT
1	1	-	-	PC0	-	TK26	S22	-	-	-	LEDPWM22	-	TxD5	(MOSI0C)/(MOSI2C)	(SDA0A)/(SDA1A)	T1PWMB	T1EX	INT00
2	2	-	-	PC1	-	TK27	S23	-	-	-	LEDPWM23	-	RxD5	(MISO0C)/(MISO2C)	-	T1PWMA	T1CAP/T1	INT01
3	3	1	27	PC2	-	TK28	S24	-	-	-	LEDPWM24	-	-	SCK0/(SCK1A)	(SCL0B)/(SCL1B)	T5PWMB	T5EX	INT02
4	4	2	28	PC3	-	TK29	S25	-	-	-	LEDPWM25	-	TxD0	MOSI0/(MOSI1A)	(SDA0B)/(SDA1B)	T5PWMA	T5CAP/T5	INT03
5	5	3	1	PC4	-	TK30	S26	-	-	-	LEDPWM26	-	RxD0	MISO0/(MISO1A)	-	-	-	INT04
6	6	4	2	PC5	-	Cmod	S27	-	-	-	LEDPWM27	-	-	-	-	-	-	INT05
7	7	5	3	VSS	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-
8	8	6	-	PC6	OSCI/32KI	TK31	-	-	-	-	-	PWM07	-	-	-	-	-	INT06
9	9	7	-	PC7	OSCO/32KO	TK32	-	-	-	-	-	PWM06	-	-	-	-	-	INT07
10	10	8	-	PC8	RST	TK33	-	-	-	-	-	PWM05	(RxD0A)	-	-	-	-	INT08
11	11	9	-	PC9	-	TK34	-	-	-	-	-	PWM04	(TxD0A)	-	-	-	-	INT09
12	-	-	-	PC10	-	TK35	-	-	-	-	-	-	-	-	-	T4PWMB	T4EX	INT10
13	-	-	-	PC11	-	TK36	-	-	-	-	-	-	-	(SCK0A)/(SCK2A)	(SCL0C)/(SCL1C)	T4PWMA	T4CAP/T4	INT11
14	-	-	-	PC12	-	TK37	-	-	-	-	-	-	(TxD4A)	(MOSI0A)/(MOSI2A)	(SDA0C)/(SDA1C)	-	-	INT12
15	-	-	-	PC13	-	TK38	-	-	-	-	-	-	(RxD4A)	(MISO0A)/(MISO2A)	-	-	-	INT13
16	12	10	4	VDD	VDD	-	-	-	-	-	-	-	-	-	-	-	-	-
17	13	11	5	PA0	FLT	-	-	-	-	-	-	-	RxD2	MISO1/(MISO2B)	-	-	-	INT00
18	14	12	6	PA1	-	-	-	-	-	CMPR	-	-	TxD2	MOSI1/(MOSI2B)	(SDA0D)/(SDA1D)	-	-	INT01
19	15	13	7	PA2	-	-	-	OP_P1	AIN15	CMP3	-	PWM03	(TxD5A)	SCK1/(SCK2B)	(SCL0D)/(SCL1D)	-	-	INT02
20	16	14	8	PA3	-	-	-	OP_P0	AIN14	CMP2	-	PWM02	(RxD5A)	-	-	-	-	INT03
21	17	15	9	PA4	-	-	-	OP_N	AIN13	CMP1	-	PWM01	(TxD2A)	-	-	-	-	INT04
22	18	16	10	PA5	-	-	-	OP_O	AIN12	CMP0	-	PWM00	(RxD2A)	-	-	-	-	INT05
23	19	-	-	PA6	-	TK0	C7	-	AIN11	-	LEDPWM28	-	-	-	-	T0PWMB	T0EX	INT06

LQFP48/QFN48	LQFP44	LQFP32/QFN32	SOP28/TSSOP28	Pin Name	Special	TK	LCD/LED	OP	ADC	CMP	LEDPWM	PWM0	UART	SPI	TWI	TnPWM	TnEX/Tn	INT
24	20	-	-	PA7	-	TK1	C6	-	AIN10	-	LEDPWM29	-	-	-	-	T0PWMA	T0CAP/T0	INT07
25	21	-	-	PA8	-	TK2	C5	-	AIN9	-	LEDPWM30	-	-	-	-	-	-	INT08
26	22	-	-	PA9	-	TK3	C4	-	AIN8	-	LEDPWM31	-	-	-	-	-	-	INT09
27	23	17	11	PA10	-	TK4	C3/S0	-	-	-	LEDPWM0	-	-	-	-	-	-	INT10
28	24	18	12	PA11	-	TK5	C2/S1	-	-	-	LEDPWM1	-	-	-	-	-	-	INT11
29	25	19	13	PA12	-	TK6	C1/S2	-	-	-	LEDPWM2	-	-	-	-	-	-	INT12
30	26	20	14	PA13	-	TK7	C0/S3	-	-	-	LEDPWM3	-	-	-	-	-	-	INT13
31	27	21	15	PA14	-	TK8	S4	-	-	-	LEDPWM4	-	-	-	-	T3PWMB	T3EX	INT14
32	28	22	16	PA15	T_CLK	TK9	S5	-	-	-	LEDPWM5	-	RxD1	(MISO0B)/(MISO1B)	-	T3PWMA	T3CAP/T3	INT15
33	29	23	17	PB0	-	TK10	S6	-	-	-	LEDPWM6	-	-	(SCK0B)/(SCK1B)	(SCL0E)/SCL1	-	-	INT00
34	30	24	18	PB1	T_DIO	TK11	S7	-	-	-	LEDPWM7	-	TxD1	(MOSI0B)/(MOSI1B)	(SDA0E)/SDA1	-	-	INT01
35	31	-	-	PB2	-	TK12	S8	-	AIN0	-	LEDPWM8	-	-	-	-	-	-	INT02
36	32	-	-	PB3	-	TK13	S9	-	AIN1	-	LEDPWM9	-	-	-	-	-	-	INT03
37	33	-	-	PB4	-	TK14	S10	-	AIN2	-	LEDPWM10	-	(RxD3A)	-	-	-	-	INT04
38	34	-	-	PB5	-	TK15	S11	-	AIN3	-	LEDPWM11	-	(TxD3A)	-	-	-	-	INT05
39	35	25	19	PB6	-	TK16	S12	-	AIN4	-	LEDPWM12	-	RxD4	-	-	-	-	INT06
40	36	26	20	PB7	-	TK17	S13	-	AIN5	-	LEDPWM13	-	TxD4	-	-	-	-	INT07
41	37	27	21	PB8	-	TK18	S14	-	AIN6	-	LEDPWM14	-	-	-	-	T2PWMB	T2EX	INT08
42	38	28	22	PB9	-	TK19	S15	-	AIN7	-	LEDPWM15	-	-	-	-	T2PWMA	T2CAP/T2	INT09
43	39	29	23	PB10	-	TK20	S16	-	-	-	LEDPWM16	-	-	-	-	T6PWMA	T6CAP/T6	INT10
44	40	30	24	PB11	-	TK21	S17	-	-	-	LEDPWM17	-	-	(SCK1C)/SCK2	SCL0/(SCL1E)	T6PWMB	T6EX	INT11
45	41	31	25	PB12	-	TK22	S18	-	-	-	LEDPWM18	-	TxD3	(MOSI1C)/MOSI2	SDA0/(SDA1E)	-	-	INT12
46	42	32	26	PB13	-	TK23	S19	-	-	-	LEDPWM19	-	RxD3	(MISO1C)/MISO2	-	-	-	INT13
47	43	-	-	PB14	-	TK24	S20	-	-	-	LEDPWM20	-	(TxD1A)	-	-	T7PWMA	T7CAP/T7	INT14
48	44	-	-	PB15	-	TK25	S21	-	-	-	LEDPWM21	-	(RxD1A)	(SCK0C)/(SCK2C)	(SCL0A)/(SCL1A)	T7PWMB	T7EX	INT15

4 Resource Diagram

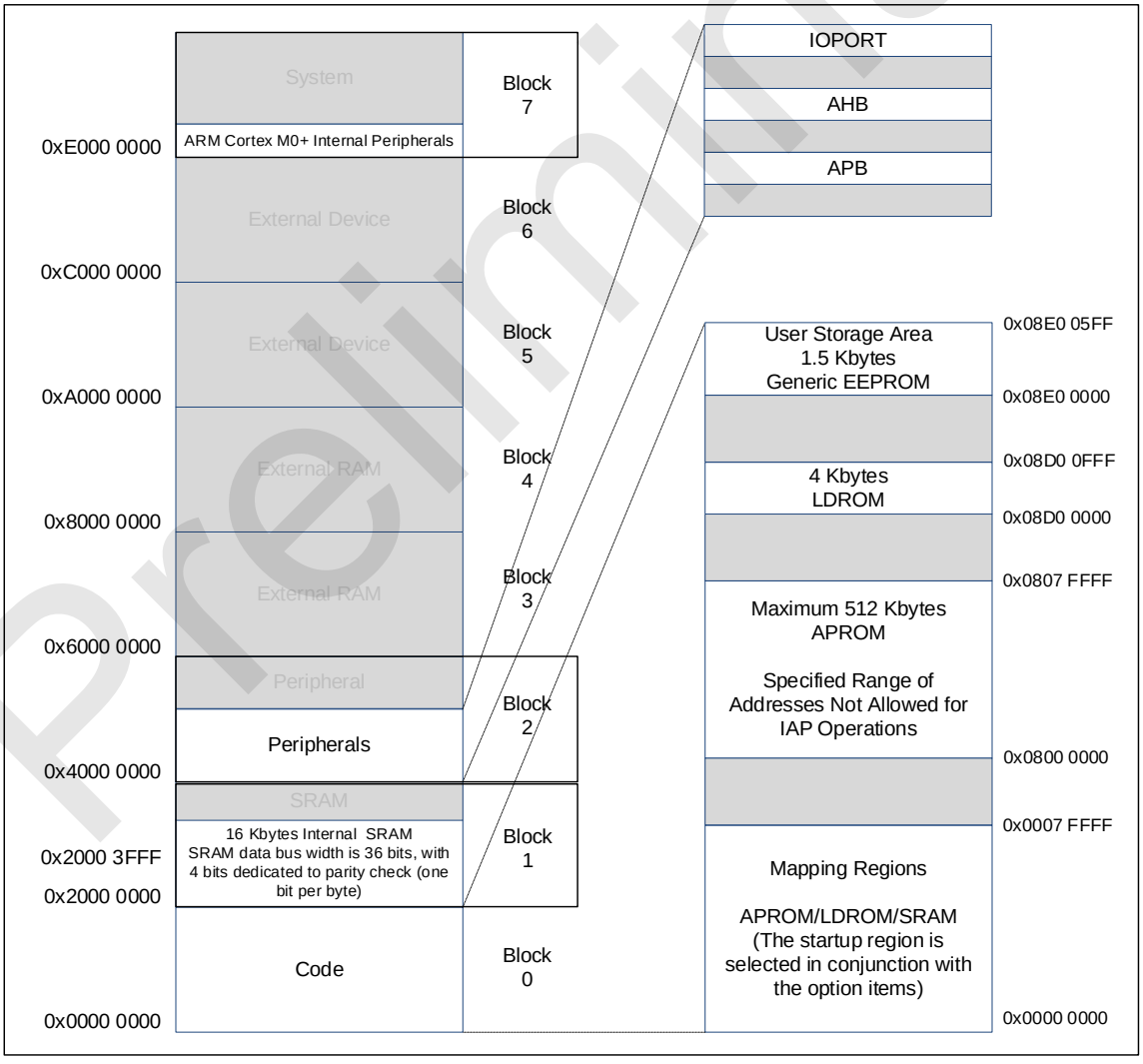


5 Flash

5.1 Overview

The program memory, data memory, and registers are arranged within a single linear (i.e., contiguous) 4 GB address space. Each byte is encoded in the storage in little-endian format, meaning that the least significant byte of a word is considered to be the lowest numbered byte, while the most significant byte is considered to be the highest numbered byte. The addressable storage space is divided into 8 main blocks, each block being 512 MB in size.

5.2 Storage Block Diagram



SC32F12T/12G Series Memory Mapping Diagram

5.3 Feature

- The Flash width is 32 bits, and it can be rewritten up to 100,000 times
- Data retention time is over 100 years at room temperature
- The structure of the Flash includes:
  - Maximum 512 Kbytes APROM
  - 4 Kbytes LDROM
  - 1.5 Kbytes user storage area (generic EEPROM)
  - 16 Kbytes Internal SRAM, support parity check
  - 96 bits Unique ID

5.4 APROM

- APROM of SC32F12xx9 series has 512Kbytes
- APROM of SC32F12xx8 series has 256Kbytes
- APROM of SC32F12xx7 series has 128Kbytes
- APROM of SC32F12xx6 series has 64Kbytes
- Sector Size: 512 bytes
- Supports: Read/Write/Sector Erase/Chip Erase/Blank Check
- The CPU (Cortex®-M0+) accesses Flash through the AHB bus
- The program defaults to booting from APROM, and users can select programs to boot from other areas such as SRAM/LDROM using the customer option OP_BL[1:0].
- Read Protection: After enabling read protection, only a program that runs from APROM can read information from APROM. Other areas or third-party tools cannot access information from APROM.
- Write Protection: Provides two hardware write protection regions where IAP operations are prohibited. Users can set the range of the two write protection regions in units of sectors based on actual needs.

The 512 Kbytes of APROM is divided into 1024 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer before writing data. During user write operations, the sector must be erased first before writing data.

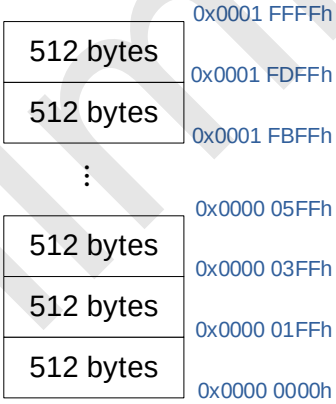
SC32F12xx9 series 512 Kbytes APROM Sector Partition Illustration

The 256 Kbytes of APROM is divided into 512 sectors, with each sector being 512 bytes. During programming, the sector to which the target address belongs will be forcibly erased by the programmer

before writing data. During user write operations, the sector must be erased first before writing data.

SC32F12xx8 series 256 Kbytes APROM Sector Partition Illustration

128 Kbytes of APROM is divided into 256 sectors, with each sector being 512 bytes. During programming, the sector corresponding to the target address is forcibly erased by the programmer before writing data. For user write operations, erasure must precede data writing.



SC32F12xx7 series 128 Kbytes APROM Sector Partition Illustration

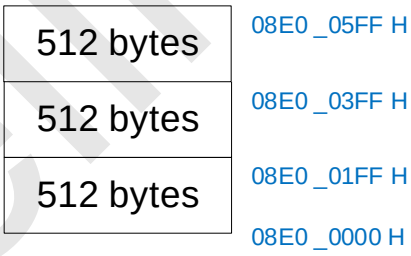
64 Kbytes of APROM is divided into 128 sectors, with each sector being 512 bytes. During programming, the sector corresponding to the target address is forcibly erased by the programmer before writing data. For user write operations, erasure must precede data writing.

SC32F12xx6 series 64 Kbytes APROM Sector Partition Illustration

5.5 1.5 Kbytes User Storage Area (Genetic EEPROM)

The 1.5K bytes of independent EEPROM area is addressed from 0x08E0_0000 H to 0x08E0_05FF H, as set by the IAPADE register. This independent EEPROM can be written to repeatedly up to 100,000 times, and it is designed to retain data for over 100 years at room temperature. The independent EEPROM supports various operations including blank check, programming, verification, erasure, and reading functions.

EEPROM has 3 sectors, with each sector being 512 bytes.



EEPROM Sector Partition Illustration

Note: The EEPROM has a write cycle endurance of 100,000 times. Users should avoid exceeding the rated write cycles of the EEPROM to prevent any anomalies!

5.6 4 Kbytes LDROM

- 4 Kbytes of system storage area, factory-programmed with BootLoader program, Users cannot modify or access this area.
- Embedded Bootloader Program: The fixed ISP program is publicly available, allowing reprogramming of Flash via UART. The program waits for upgrade commands, and if no update command is received within 500 milliseconds, it jumps to APROM for execution (0X8000 0000).

5.6.1 BootLoader

Supports two Bootloader modes:

- Software Approach: Directly partition BootLoader and APP areas in software. Easy sharing interrupts of BootLoader and APP by modifying VTOR. Flexible adjustment of the size of each area；
- Hardware Approach: 4 Kbytes fixed "LDROM" as a dedicated BootLoader area that users cannot read or write
  - LDROM serves as a fixed BootLoader space with factory-programmed program, and users cannot read or write
  - Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

5.7 SRAM

- Internal SRAM：16 Kbytes，address 0x2000 0000 ~ 0x2000 3FFF
- Supports parity check
  - An additional 2K RAM is used for parity checking, which means SRAM data bus width is 36 bits, with 4 bits dedicated to parity check (one bit per byte).
  - The parity check bits are calculated and saved when writing to the SRAM, and automatically verified upon reading. If a bit fails, an unmaskable interrupt (Cortex®-M0+ NMI) will be generated.
  - Provides an independent SRAM parity error flag, SRAMPEIF.

Note: When SRAM parity check is enabled, it is recommended to perform a software initialization of the entire SRAM at the beginning of the code to prevent parity check errors when reading from uninitialized locations.

- Users can choose to start the program from SRAM by configuring the customer option OP_BL[1:0].
- It supports byte, half-word (16-bit), or word (32-bit) access at the maximum system clock frequency, with no waiting states. Therefore, it can be accessed by both the CPU and DMA

5.8 Boot Area Selection (Bootstrap)

After a reset, users can independently configure the desired bootstrap mode.

After exiting the standby mode, the startup mode configuration can be resampled. Once this startup delay has ended, the CPU will fetch the stack top value from address 0x00000000 and then begin executing code from the bootstrap memory starting at 0x00000004.

There are three options for bootstrap area selection: Main Flash Memory Area, System Flash Memory Area and SRAM, described in detail as follows:

5.8.1 Bootstrap from APROM

APROM is aliased in the bootstrap memory space (0x00000000) but can also be accessed from its original memory space (0x08000000). In other words, the program can start accessing from either address 0x00000000 or 0x08000000.

5.8.2 Bootstrap from LDROM

- 4 Kbytes LDROM serves as a fixed BootLoader space with factory-programmed program, Users cannot modify or access this area.
- Embedded Bootloader Program: The embedded bootloader program resides in LDROM and is programmed during the production stage. The fixed ISP program is publicly available, allowing reprogramming of Flash via UART.

5.8.3 Bootstrap from SRAM

SRAM has an alias in the bootstrap memory space (0x0000 0000) but can also be accessed from its original memory space (0x2000 0000).

5.8.4 Bootstrap mode config

The bootstrap modes can be controlled by the register bits BTLD[1:0] in conjunction with the software reset (RST) control bit, both protected by the IAP_KEY:：

① Set BTLD[1:0]=0x00: the chip boots from APROM after a software reset

② Set BTLD[1:0]=0x01: the chip boots from LDROM after a software reset

③ Set BTLD[1:0]=0x10: the chip boots from SRAM after a software reset

The initial boot region selection during power-up can be configured by customer option bits OP_BL[1:0]:

① Set OP_BL[1:0]=0x00: the chip boots from APROM after a software reset

② Set OP_BL[1:0]=0x01: the chip boots from LDROM after a software reset

③ Set OP_BL[1:0]=0x10: the chip boots from SRAM after a software reset

5.9 96 bits Unique ID

The SC32F12T/12G provides an independent Unique ID area. A 96-bit unique code can be pre-programmed before leaving the factory to ensure the uniqueness of the chip. The only way for the user to obtain the serial number is to read through the IAP instruction.

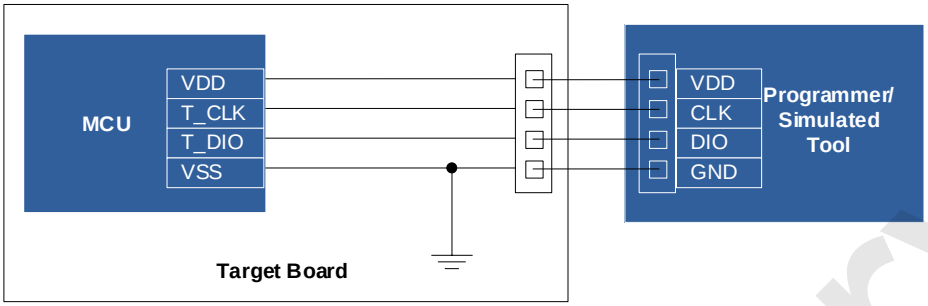
5.10 User ID Area

User ID area, where user-costomized ID is pre-programmed when leaving the factory. Users can read the User ID area, but cannot write the User ID area.

5.11 Programming

The SC32F12T/12G's Flash can be programmed through T_DIO, T_CLK, VDD, VSS, the specific connection

relationship is as follows:



ICP mode Flash Writer programming connection diagram

T_DIO、T_CLK is a 2-wire JTAG programming and emulation signal line. Users can configure the mode of these two ports through the Customer Option when programming.

5.11.1 JTAG Specific Mode

T_DIO,T_CLK are specific port for programming and emulation, and other functions multiplexed with it are not available. This mode is generally used in the online debugging stage, which is convenient for users to simulate and debug. After the JTAG special mode takes effect, the chip can directly enter the programming or emulation mode without powering on and off again.

5.11.2 Normal Mode (JTAG specific port is invalid)

The JTAG function is not available, and other functions multiplexed with it can be used normally. This mode can prevent the programming port from occupying the MCU pins, which is convenient for users to maximize the use of MCU resources.

Note: When the invalid configuration setting of the JTAG dedicated port is successful, the chip must be completely powered off and then on again to enter the programming or emulation mode, which will affect the programming and emulation in the live mode. SinOne recommends that users select the invalid configuration of the JTAG dedicated port during mass production and programming, and select the JTAG mode during the development and debugging phase.

Related Customer Option is as followed:

Register	R/W	Description	Reset Value
COPT1_CFG@0xC2	R/W	Customer Option Mapping Register 1	0x0000_0000

7	6	5	4	3	2	1	0
ENWDT	DISJTG	DISRST	-	-	-	OP_BL[1:0]	

Bit number	Bit Mnemonic	Description
6	DISJTG	JTAG Ports Switch Control Bit 0: JTAG mode enabled, the corresponding pins can only be used as T_CLK and T_DIO 1: Normal mode, JTAG function disabled

5.12 Security Encryption

- The SC32F12T/12G series mainly involves encrypting the APROM for read protection. Users can configure the read protection encryption feature during programming through the customer option in the dedicated programming host; enable flash read protection can enter encryption mode: The chip defaults to a non-encrypted state while leaving the factory
- The read protection encryption feature has no mapped registers. Users can only modify it after config the customer option in the dedicated programming host and programming.
- Encryption Disabled: Operations such as reading, programming, and erasing can be performed on APROM. These operations can be also performed on Bytes and backup registers.
- Encryption Enabled:
  - Enable from APROM: Code executed in user mode (booting from user APROM) can perform all operations on APROM.
  - Debug, enable from SRAM and LDROM: In debug mode or when code is booted from SRAM or LDROM, APROM is completely inaccessible.
- Disabling encryption requires a full erase operation on APROM.

5.12.1 Security Encryption Access Rights

Boot Area/Tools	Encryption Disabled Status					Read Protection Encryption Status				
	Read	Write	Block Earse	Full Earse	Operate Write-Protection Region	Read	Write	Block Earse	Full Earse	Operate Write-Protection Region
Bootstrap from APROM	√	√	√	\	Forbid	√	√	√	\	Forbid
Debug/Bootstrap from SRAM	√	√	√	√	Forbid	Forbid	Forbid	Forbid	Forbid	Forbid
Bootstrap from LDROM	√	√	√	√	√	Forbid	Forbid	Forbid	√	Forbid

5.13 In Application Programming (IAP)

The IAP (In Application Programming) area in the APROM of SC32F12T/12G allows users to perform remote program updates through IAP operations. Users can also retrieve information from the Unique ID or User ID areas by IAP read operations. Before performing IAP write operations, users must carry out sector erasure for the target address sector.

The chip allows global IAP operations in the APROM by default while leaving the factory. Internally, the chip

provides two sets of flash write protection regions. These regions are set based on sector units, and the protected areas are restricted from IAP operations. The rules for setting these regions are as follows:

IAPPORx Register Value（x=A or B）	IAPPOR Protection Area
IAPPORx_ST = IAPPORx_ED	Sector IAPPORx
IAPPORx_ST > IAPPORx_ED	No protection
IAPPORx_ST < IAPPORx_ED	Sectors from IAPPORx_ST to IAPPORx_ED

User can config these APROM's write protection area through "Customer Option" while programming.

Note: IAP does not support byte or half-word programming. That is, when writing to memory using IAP, the data must be word-aligned (aligned on a 4-byte boundary). If data is written on a byte or half-word boundary, it will automatically be repeated to fill the entire word. For example, when writing 0x12, it will be automatically padded to 0x1212_1212 before being written; when writing 0x1234, it will be automatically padded to 0x1234_1234 for the write operation.

6 Power,Reset And System Clock（RCC）

6.1 Power-on Reset

After the SC32F12T/12G power-on, the processes carried out before execution of client software are as follows:

① Reset stage
② Loading information stage
③ Normal operation stage

6.1.1 Reset Stage

The SC32F12T/12G will always be reset until the voltage supplied to SC32F12T/12G is higher than a certain voltage, and the internal Clock starts to be effective. The duration of reset stage is related to rising speed of external power. Once the external supply voltage is up to built-in POR voltage, the reset stage would be completed.

6.1.2 Loading Information Stage

There is a warm-up counter inside The SC32F12T/12G. During the reset stage, the warm-up counter is cleared to 0 until the voltage exceeds the POR voltage, the built-in HIRC oscillator starts to oscillate, and the warm-up counter starts counting. When the internal warm-up counter counts to a certain number, every certain number of HIRC clocks will read a byte of data from the IFB (including Customer Option) in the Flash ROM and store it in the internal system register. This reset signal will not end until the warm-up is completed.

6.1.3 Normal Operation Stage

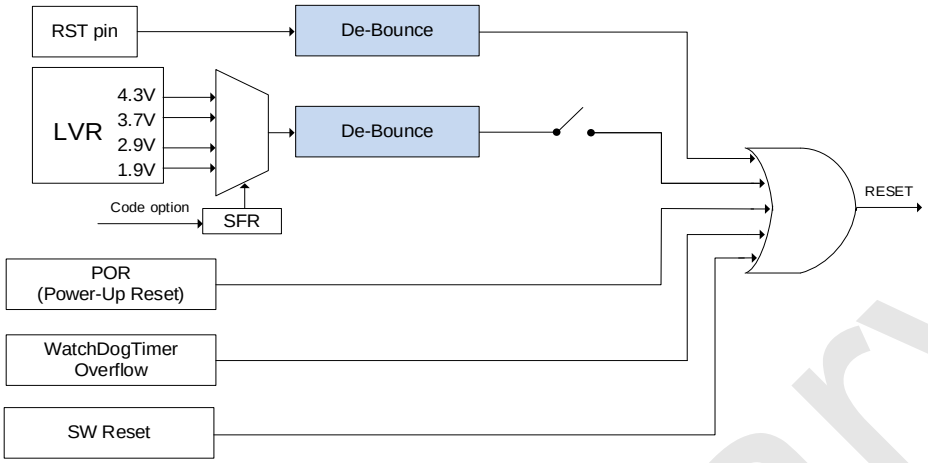
After finishing the Loading Information stage, The SC32F12T/12G starts to read the instruction code from Flash and enters the normal operation stage. The LVR voltage is the set value of Customer Option written by the user.

6.2 Reset Modes

The SC32F12T/12G has 5 reset methods, the first four are hardware reset:

- External reset
- Low-voltage reset LVR
- Power-on reset POR
- Watchdog WDT reset
- Software reset

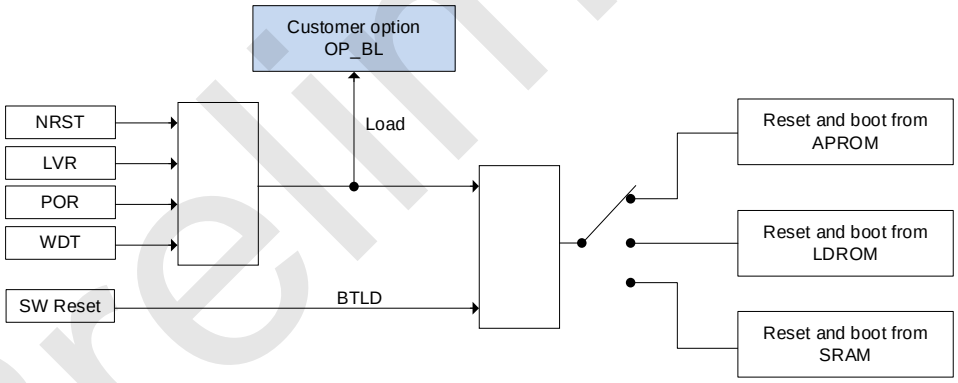
The circuit diagram of the reset part of the SC32F12T/12G is as follows:



SC32F12T/12G Reset Circuit Diagram

6.2.1 Boot area after the reset

After hardware reset through external RST, low voltage reset (LVR), power-on reset (POR), or watchdog reset (WDT), the chip boots from the startup area (APROM / LDROM / SRAM) set by the user in OP_BL. After the software reset, the chip boots from the startup area (APROM / LDROM / SRAM) set by BTLD[1:0].



SC32F12T/12G Boot Area Switching diagram after reset

6.2.2 External RST

External reset is a low-level reset pulse signal of a certain width given to SC32F12T/12G from external RST pin to realize the reset of SC32F12T/12G. User can configure the PC8/NRST pin as RST (reset pin) using the programming host software by Customer Option before programming.

6.2.3 Low-voltage Reset LVR

The SC32F12T/12G provides a low-voltage reset circuit. There are 4-level LVR voltage options: 4.3V, 3.7V, 2.9V, 1.9V. The default value is the Customer Option value written by the user. A reset occurs when the VDD voltage is less than the threshold voltage for low-voltage reset and the duration is greater than T_{LVR}. Among them, T_{LVR} is the buffeting time of LVR, about 30μs.

6.2.4 Power-on Reset(POR)

The SC32F12T/12G has a power-on reset circuit inside. When the power supply voltage V_{DD} reaches the POR reset voltage, the system automatically resets.

6.2.5 Watchdog Reset(WDT)

The SC32F12T/12G has a WDT, the clock source of which is the built-in 32 kHz oscillator. The user can choose whether to enable the watchdog reset function by Customer Option.

6.2.6 Software Reset

Enable RST(IAP_CON.8) will immediately reset the system.

6.2.7 Initial Reset State

When SC32F12T/12G is in the reset state, most registers return to their initial state. The watchdog (WDT) is in the disabled state. 'Hot-start' resets (such as WDT, LVR, software reset, etc.) do not affect SRAM, and SRAM values remain the same as before the reset. Loss of SRAM content occurs when the power supply voltage drops to a level where RAM cannot retain data.

6.3 Clock

6.3.1 System Clock Source

Four different clock sources can be used to drive the system clock (SYSCLK):

- Built-in high-frequency 64MHz oscillator (HIRC)
- External high-frequency crystal oscillator (HXT)
- Built-in low-frequency 32KHz oscillator (LIRC)
- External low-frequency crystal oscillator (LXT)

Note：

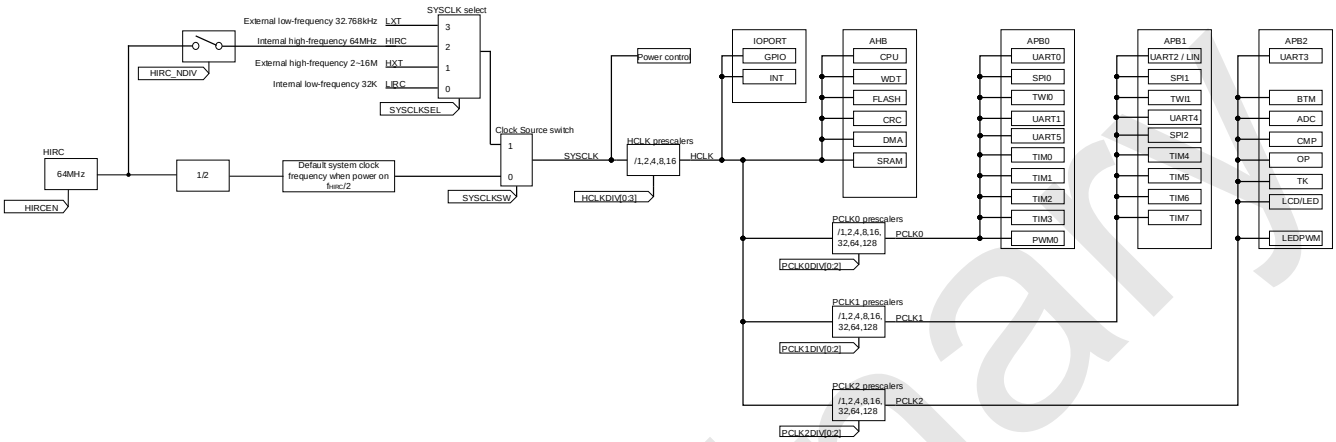
1. **The default system clock source at power-up is HIRC, and it's frequency is f_{HIRC}/2. Users can switch the clock source through software during normal operation after power-up. Before switching, ensure that the selected clock source is in a stable operating state.**
2. **Regardless of the chosen clock source to switch to, the system clock source must first be switched to HIRC before transitioning to the target clock source.**

6.3.2 Bus

- Users can configure the frequencies of the AHB, APB0, APB1, and APB2 domains through multiple prescalers. HCLK: The main clock of the AHB domain, with a maximum frequency of 64MHz. It drives components such as the Cortex®-M0+ core, memory, and DMA.
- PCLK0: The main clock of the APB0 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB0 bus are driven by PCLK0.
- PCLK1: The main clock of the APB1 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB1 bus are driven by PCLK1.
- PCLK2: The main clock of the APB2 domain, with a maximum frequency equal to the HCLK frequency. Peripheral devices on the APB2 bus are driven by PCLK2.

The RCC divides the AHB clock (HCLK) by 8 to serve as the external clock for SysTick. By setting the control and status registers of SysTick, you can choose either the above-mentioned clock or the core clock as the SysTick clock source.

6.3.3 Clock and Bus Allocation Block Diagram



Clock and Bus Allocation Block Diagram

Note: Default system clock frequency when power on "f_{SYS}" is $f_{HIRC/2}$, users can change clock source by modify SYSCLKSW or SYSCLKSEL.

6.4 RCC Interrupt

In coordination with the stop oscillation detection mechanism, SC32F12T/12G's clock source provides a user-configurable RCC interrupt: when the system clock source is LXT/HXT, if an abnormality is detected in the clock source, the stop oscillation detection interrupt flag will be set. If the corresponding interrupt is enabled at this point, a stop oscillation detection interrupt will be generated.

6.5 Built-in high-frequency 64MHz Oscillator (HIRC)

- Can be selected as the system operating clock
- Default system clock frequency when power on "f_{SYS}" is $f_{HIRC/2}$
- Frequency error: Within ±1% @ -40 ~ 105℃ @ 2.0V~ 5.5V
- The system clock can be automatically calibrated by 32.768 kHz external crystal oscillator, after calibration HIRC accuracy can be infinitely close to the accuracy of external 32.768 kHz crystal oscillator

6.6 External High-Frequency Crystal Oscillator Circuit, Can Connect to 2~16MHz Oscillator (HXT)

- Can be selected as the system operating clock
- Can be externally connected to a 2~16MHz high-frequency oscillator

6.7 Built-in Low-Frequency 32kHz Oscillator (LIRC)

- Can be selected as the system operating clock
- Can be selected as the LCD/LED clock source
- Can be selected as the Base Timer and WDT clock source
- Frequency error: Within ±4% @ -20 ~ 85℃ @ 4.0V~ 5.5V, after register correction

6.8 External Low-Frequency Oscillator Circuit, Can Connect to 32.768kHz Oscillator (LXT)

- Can be selected as the system operating clock
- Can be selected as the Base Timer clock source
- Can be selected as the LCD/LED clock source
- Allows for an external 32.768kHz low-frequency oscillator
- Automatic calibration of HIRC can be performed using LXT

7 Interrupts

- M0+ core could provide a maximum of 32 interrupt sources, numbered from 0 to 31, while SC32F12T/12G series has 25 interrupt sources.
- Four-level interrupt priorities can be configured, and the interrupt priorities are set through the Interrupt Priority Registers in the core registers.

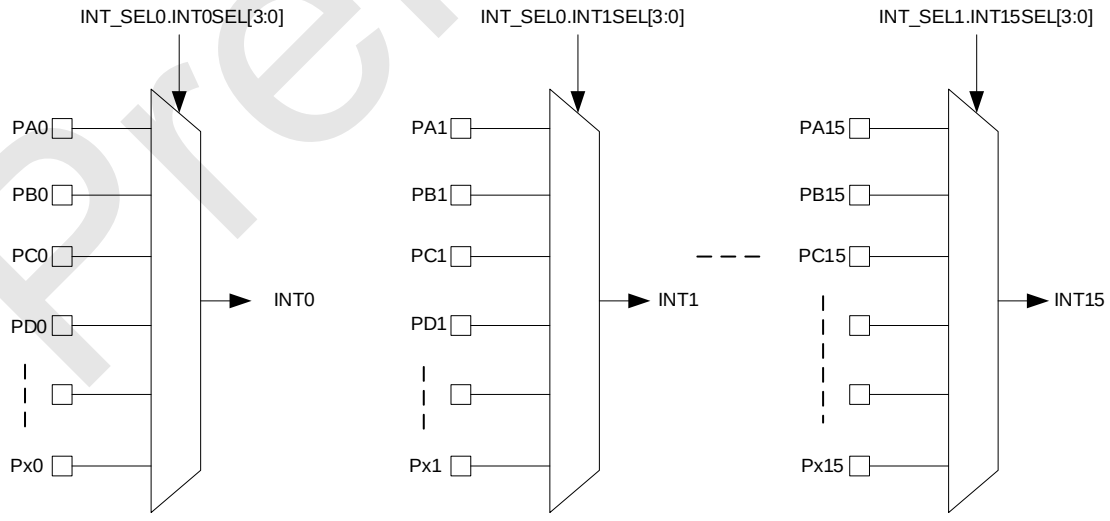
7.1 External interrupts INT0~15

External interrupts comprise 16 interrupt sources, occupying a total of 4 interrupt vectors. All 16 external interrupt sources can be configured to respond to rising edges, falling edges, or both edges. Once configured, these interrupts can cover all GPIO pins. When the corresponding event occurs, software sets the corresponding interrupt flag (RIF/FIF to 1), triggering entry into the corresponding interrupt service.

The external interrupt features of the SC32F12T/12G series are as follows:

- 16 INT interrupt sources, occupying 4 interrupt vectors in total.
- After configuration, INT can cover all GPIO pins.
- All INT sources can be configured for rising edge, falling edge, or both edge interrupts, each having independent corresponding interrupt flag.
- Software sets the corresponding interrupt flag can trigger entry into the corresponding interrupt service.

Note: When using INT functions, users need to manually set the GPIO port corresponding to INTn (n=0~15) to pull-up input mode. External interrupts cannot be detected in output mode.



External Interrupt Port Multiplexer

7.2 Interrupt and Events

- When NVIC is disabled, interrupt request masks are enabled, events can be generated, but interrupt

cannot be generated.

- When NVIC is enabled, interrupt request masks act as internal master interrupt control bit in the module.

7.3 Interrupt Source and Vector

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
0	-	-	0x0000_0000	-		-	\	\	YES
1	-	Fixed	0x0000_0004	RESET	PRIMASK	SCB	\	\	YES
2	-	Fixed	0x0000_0008	NMI_Handler		SCB	\	\	YES
3	-	Fixed	0x0000_000C	HardFault_Handler	PRIMASK	SCB	\	\	YES
4~10	-	-	0x0000_0010 - 0x0000_0028	-		-	\	\	YES
11	-	Settable		SVC_Handler	PRIMASK	SCB	\	\	YES
12~13	-	-	0x0000_0030 0x0000_0034	-		-	\	\	YES
14	-	Settable	0x0000_0038	PendSV_Handler	PRIMASK	SCB	\	\	YES
15	-	Settable	0x0000_003C	SysTick_Handler	PRIMASK	SysTick_CTRL	\	\	YES
16	0	Settable	0x0000_0040	INT0	NVIC->ISER[0].0	INTF_IE->ENFx，x=0 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
17	1	Settable	0x0000_0044	INT1-7	NVIC->ISER[0].1	INTF_IE->ENFx，x=1~7 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
18	2	Settable	0x0000_0048	INT8-11	NVIC->ISER[0].2	INTF_IE->ENFx，x=8~11 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
19	3	Settable	0x0000_004C	INT12-15	NVIC->ISER[0].3	INTF_IE->ENFx， x=12~15 INTR_IE->ENRx	\	INTF_STS->FIFx INTR_STS->RIFx	YES
20	4	Settable	0x0000_0050	RCC 停振检测	NVIC->ISER[0].4	RCC_CFG->INTEN	\	RCC_STS->CLKFIF	YES
21	5	Reserved	0x0000_0054	\	NVIC->ISER[0].5	\	\	\	
22	6	Settable	0x0000_0058	BTM	NVIC->ISER[0].6	BTM_CON->INTEN	\	BTM_STS->BTMIF	YES
23	7	Settable	0x0000_005C	UART0	NVIC->ISER[0].7	UART0_IDE->INTEN	UART0_IDE->TXIE UART0_IDE->RXIE	UART0_STS->TXIF UART0_STS->RXIF	YES
				UART2/LIN	\	UART2_IDE->INTEN	UART2_IDE->TXIE UART2_IDE->RXIE UART2_IDE->BKIE UART2_IDE->SLVHEIE	UART2_STS->TXIF UART2_STS->RXIF UART2_STS->BKIF UART2_STS->SLVHEIF	NO
				UART4	\	UART4_IDE->INTEN	UART4_IDE->TXIE UART4_IDE->RXIE	UART4_STS->TXIF UART4_STS->RXIF	YES
24	8	Settable	0x0000_0060	UART1	NVIC->ISER[0].8	UART1_IDE->INTEN	UART1_IDE->TXIE UART1_IDE->RXIE	UART1_STS->TXIF UART1_STS->RXIF	YES

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
				UART3	\	UART3_IDE->INTEN	UART3_IDE->TXIE UART3_IDE->RXIE	UART3_STS->TXIF UART3_STS->RXIF	YES
				UART5	\	UART5_IDE->INTEN	UART5_IDE->TXIE UART5_IDE->RXIE	UART5_STS->TXIF UART5_STS->RXIF	YES
25	**9**	Settable	0x0000_0064	SPI0	NVIC->ISER[0].9	SPI0_IDE->INTEN	SPI0_IDE->RXNEIE SPI0_IDE->TBIE SPI0_IDE->RXIE SPI0_IDE->RXHIE SPI0_IDE->TXHIE	SPI0_STS->SPIF SPI0_STS->RXNEIF SPI0_STS->TXEIF SPI0_STS->RXFIF SPI0_STS->RXHIF SPI0_STS->TXHIF	NO
26	**10**	Settable	0x0000_0068	SPI1	NVIC->ISER[0].10	SPI1_IDE->INTEN	\	SPI1_STS->SPIF SPI1_STS->TXHIF	NO
				SPI2		SPI2_IDE->INTEN	\	SPI2_STS->SPIF SPI2_STS->TXEIF	NO
27	**11**	Settable	0x0000_006C	DMA0	NVIC->ISER[0].11	DMA0_CFG->INTEN	DMA0_CFG->TCIE DMA0_CFG->HTIE DMA0_CFG->TEIE	DMA0_STS->GIF DMA0_STS->TCIF DMA0_STS->HTIF DMA0_STS->TEIF	NO
28	**12**	Settable	0x0000_0070	DMA1	NVIC->ISER[0].12	DMA1_CFG->INTEN	DMA1_CFG->TCIE DMA1_CFG->HTIE DMA1_CFG->TEIE	DMA1_STS->GIF DMA1_STS->TCIF DMA1_STS->HTIF DMA1_STS->TEIF	NO
29	**13**	Reserved	0x0000_0074	\	NVIC->ISER[0].13	\	\	\	NO
30	**14**	Reserved	0x0000_0078	\	NVIC->ISER[0].14	\	\	\	NO
31	**15**	Settable	0x0000_007C	TIM0	NVIC->ISER[0].15	TIM0_IDE->INTEN	TIM0_IDE->TIE TIM0_IDE->EXFIE TIM0_IDE->EXRIE	TIM0_STS->TIF TIM0_STS->EXIF TIM0_STS->EXIR	NO
32	**16**	Settable	0x0000_0080	TIM1	NVIC->ISER[0].16	TIM1_IDE->INTEN	TIM1_IDE->TIE TIM1_IDE->EXFIE TIM1_IDE->EXRIE	TIM1_STS->TIF TIM1_STS->EXIF TIM1_STS->EXIR	NO
33	**17**	Settable	0x0000_0084	TIM2	NVIC->ISER[0].17	TIM2_IDE->INTEN	TIM2_IDE->TIE TIM2_IDE->EXFIE TIM2_IDE->EXRIE	TIM2_STS->TIF TIM2_STS->EXIF TIM2_STS->EXIR	NO
34	**18**	Settable	0x0000_0088	TIM3	NVIC->ISER[0].18	TIM3_IDE->INTEN	TIM3_IDE->TIE TIM3_IDE->EXFIE TIM3_IDE->EXRIE	TIM3_STS->TIF TIM3_STS->EXIF TIM3_STS->EXIR	NO
35	**19**	Settable	0x0000_008C	TIM4	NVIC->ISER[0].19	TIM4_IDE->INTEN	TIM4_IDE->TIE TIM4_IDE->EXFIE TIM4_IDE->EXRIE	TIM4_STS->TIF TIM4_STS->EXIF TIM4_STS->EXIR	NO

Interrupt Vector	Interrupt Number	Priority	Interrupt Vector Address	Interrupt Source	Core/NVIC Enable Bit	Interrupt Request Mask Bit	Interrupt Subroutine Control Bit	Interrupt Flag	Capability of Waking up STOP
				TIM5	\	TIM5_IDE->INTEN	TIM5_IDE->TIE TIM5_IDE->EXFIE TIM5_IDE->EXRIE	TIM5_STS->TIF TIM5_STS->EXIF TIM5_STS->EXIR	NO
36	20	Settable	0x0000_0090	TIM6	NVIC->ISER[0].20	TIM6_IDE->INTEN	TIM6_IDE->TIE TIM6_IDE->EXFIE TIM6_IDE->EXRIE	TIM6_STS->TIF TIM6_STS->EXIF TIM6_STS->EXIR	NO
				TIM7	\	TIM7_IDE->INTEN	TIM7_IDE->TIE TIM7_IDE->EXFIE TIM7_IDE->EXRIE	TIM7_STS->TIF TIM7_STS->EXIF TIM7_STS->EXIR	NO
37	21	Settable	0x0000_0094	PWM0	NVIC->ISER[0].21	PWM0_CON->INTEN	\	PWM0_STS->PWMIF	NO
38	22	Settable	0x0000_0098	LEDPWM	NVIC->ISER[0].22	LEDPWM_CON->INTEN	\	LEDPWM_STS->PWMIF	NO
39	23	Settable	0x0000_009C	TWI0	NVIC->ISER[0].23	TWI0_IDE->INTEN	\	TWI0_STS->TWIF	NO
40	24	Settable	0x0000_00A0	TWI1	NVIC->ISER[0].24	TWI1_IDE->INTEN	\	TWI1_STS->TWIF	NO
41	25	Reserved	0x0000_00A4	\	\	\	\	\	
42	26	Reserved	0x0000_00A8	\	\	\	\	\	
43	27	Reserved	0x0000_00AC	\	\	\	\	\	
44	28	Reserved	0x0000_00B0	\	\	\	\	\	
45	29	Settable	0x0000_00B4	ADC	NVIC->ISER[0].29	ADC_CON->INTEN	\	ADC_STS->ADCIF	NO
46	30	Settable	0x0000_00B8	CMP	NVIC->ISER[0].30	CMPCFG->CMPIM[1:0]	\	CMP_STS->CMPIF	YES
47	31	Settable	0x0000_00BC	TK	NVIC->ISER[0].31	TKCON->INTEN	\	TKCON->TKIF	YES

8 Power Saving Mode

Upon initial power-up, the system runs in Normal Mode. Additionally, three power-saving modes are available:

- Low-Speed Mode: The system clock source can be LIRC, and the CPU can operate at 32KHz.
- IDLE Mode: The system can be awakened by any interrupt.
- STOP Mode: The system can be awakened by INT0~15, Base Timer, TK, and CMP.

9 GPIO

9.1 Clock Source

M0+ core can achieve single-cycle access to GPIO through the IOPORT bus, resulting in highly efficient data transfer. The IOPORT bus clock is derived from HCLK.

9.2 Feature

The GPIO port features of the SC32F12T/12G series are as follows:

- A maximum of 46 bidirectional independently controlled GPIOs
- CPU can access GPIO ports through the IOPORT bus in a single cycle
- Independent setting of pull-up resistors
- All ports have four levels of source driving capability
- All I/Os have high sink current driving capability (50mA)
- 16 I/Os in one group
- Whether input mode or output mode, reading from the port data register retrieves the actual status value of the port

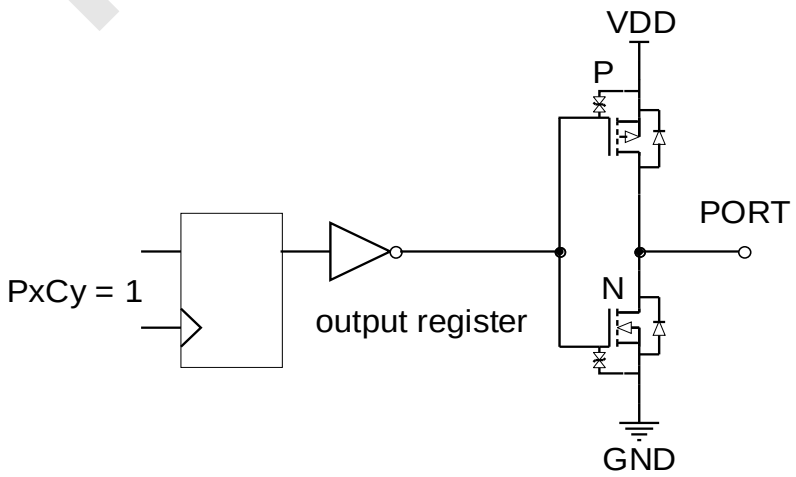
Note: Unused and non-exported ports should be set to strong push-pull output mode

9.3 GPIO Structure Diagram

Strong Push-pull Output Mode

In the strong push-pull output mode, it can provide continuous high-current drive: For detailed electrical parameters, please refer to the "GPIO Parameters" section.

The schematic diagram of the port structure of the strong push-pull output mode is as follows:

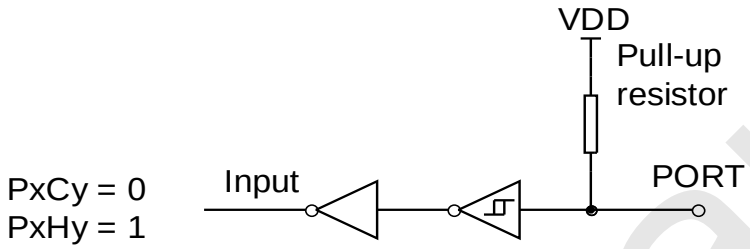


Strong push-pull output mode

Pull-up Input Mode

In the pull-up input mode, a pull-up resistor is constantly connected to the input port. Only when the input port is pulled low, the low-level signal is detected.

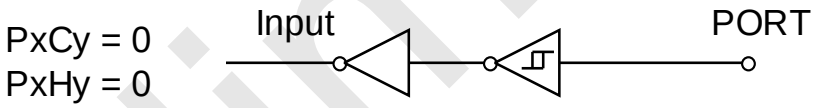
The schematic diagram of the port structure with pull-up input mode is as follows:



Input mode with pull-up resistor

High Impedance Input Mode (Input only)

The schematic diagram of the port structure of the high impedance input mode is as follows:



High impedance input mode

10 Analog-to-Digital Converter ADC

10.1 Clock source

- The SC32F12T/12G series ADC has only one clock source, which is derived from PCLK
- Fixed conversion time of 950ns

10.2 Feature

- Precision：14 bits
- Maximum Channels: Supports up to 18 channels:
  - 16 external ADC sampling channels and other functions multiplexed with I/O ports.
  - 1 internal ADC channel can directly measure the VDD voltage
  - 1 internal ADC channel can directly measure the OP output
- Built-in Reference Voltages: 2.4V,2.048V, and 1.024V
- Reference Voltage Selection: VDD,2.4V,2.048V and 1.024V
- Direct Measurement of VDD: The internal ADC can directly measure the VDD voltage
- ADC Input Channel Selection: Can be configured through the ADCIS[4:0] bits.
- Software-Triggered Conversion: The conversion process can be initiated by software
- Interrupt Support: Configurable ADC conversion completion interrupt
- Conversion Time: Sampling to completion time as low as 2μs
- DMA Transfer Support: ADC conversion completion can generate a DMA request
- Single-Channel Continuous Conversion Mode Support: Allows continuous conversion in single-channel mode
- Overflow Flag: The ADC conversion result supports an overflow flag, and the OVERRUN flag is in the same register (ADCV), allowing the user to read both at once

10.3 ADC Conversion Steps

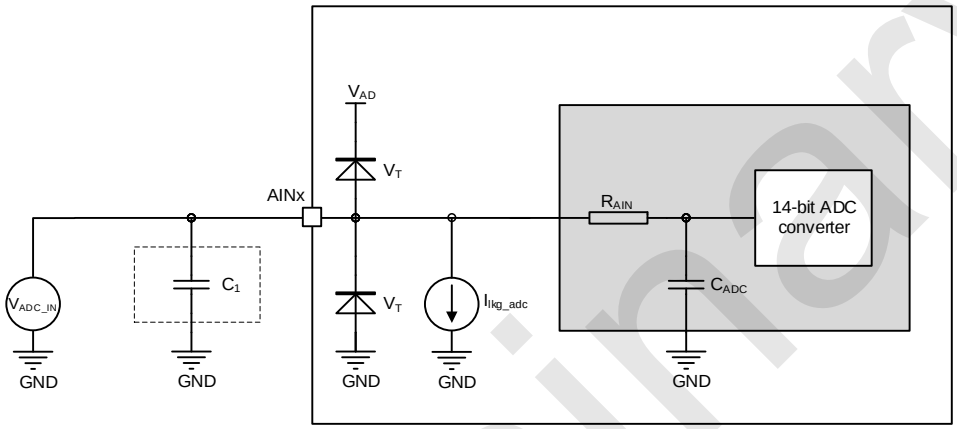
The actual operation steps required for the user to perform ADC conversion are as follows:

① Set the ADC input pin; (set the bit corresponding to AINx as ADC input, usually the ADC pin will be fixed in advance);
② Set ADC reference voltage Vref, set the frequency used for ADC conversion;
③ Set ADCEN to enable the ADC module power supply;
④ Select ADC input channel; (set ADCIS bit, select ADC input channel);
⑤ Start ADCS and start conversion;
⑥ Wait for EOC/ADCIF=1. If the ADC interrupt is enabled, the ADC interrupt will be generated. The user needs to clear the EOC/ADCIF flag by software;
⑦ Get 14-bit data from ADCV, then one conversion is completed;
⑧ If the input channel is not changed, continuous conversion mode can be set by setting CONT to 1 through software. The conversion will continue until this bit is cleared to 0;
⑨ When the ADC conversion result overflows, the OVERRUN flag will set to 1;

⑩ Conversion data can be transferred using DMA;

Note: Before setting the ADC_CON[8] bit, it is recommended that users first clear the EOC/ADCIF using software. Additionally, after the ADC interrupt service routine has been executed, the EOC/ADCIF should also be cleared to prevent continuous generation of ADC interrupts.

10.4 ADC Structure Diagram



Note:

1. **C1 is an external 0.01μF capacitor. Users are advised to add this capacitor to improve the performance of the ADC.**
2. **For detailed electrical parameters related to the ADC, please refer to Section 26.10 ADC Characteristics.**

11 Operational Amplifier(OP)

11.1 Overview

A built-in internal operational amplifier and programmable gain amplifier, offering a rail-to-rail input stage. The OP can be configured in PGA mode, featuring 5 non-inverting input terminals, 2 inverting input terminals, and 3 output terminals. It provides options for 8/16/32/64 times non-inverting gain and 7/15/31/63 times inverting gain.

11.2 Feature

- A rail-to-rail input stage
- Can be configurable as a Programmable Gain Amplifier (PGA)
  - Non-inverting gain: 8/16/32/64
  - Inverting gain: 7/15/31/63
- Two external pins for the non-inverting input: OP_P0 or OP_P1
- One external pin for the inverting input: OP_N
- One external pin for the output: OP_O
- The output can be directly connected to the ADC input
- The output can be directly connected to the positive input of a Comparator (CMP)
- Precision adjustment can be achieved by setting the PGA input offset control bit PGAOFC to 1, which will short the positive and negative input terminals of the OP (operational amplifier) module

11.3 OP Port Selection

11.3.1 OP Positive Input Selection

The positive input terminal of OP module can be switched and selected by OPPSEL[2:0], and it has five options:

- OP_P0 external pin
- OP_P1 external pin
- Internal VSS
- Internal 1.2V reference
- VDD

11.3.2 OP Negative Input Selection

The negative input terminal of the OP module has two options:

- OP_N external pin.

When choosing the OP_N external pin as the negative input for the OP, the OP input control bit OPNSEL should be set to 0, and the feedback resistor selection bits FDBRSEL[1:0] should be set to 01.

- Internal feedback resistor.

When choosing the internal feedback resistor as the negative input for the OP, the OP input control bit OPNSEL should be set to 1, and the feedback resistor selection bits FDBRSEL[1:0] should be set to 00, 11, or 10, and the internal gain can be selected by internal gain selection bits PGAGAN[1:0].

11.3.3 OP Output Selection

The output of the OP module has three options:

- Sampling channel of the AD converter

When OP is used as an ADC input, users should set ENOP=1 to enable the OP module, then set ADCEN=1 to power on the ADC. The conversion result of OP can be directly obtained in the ADCV register by selecting the OP output port as the ADC input port through ADCIS[4:0].

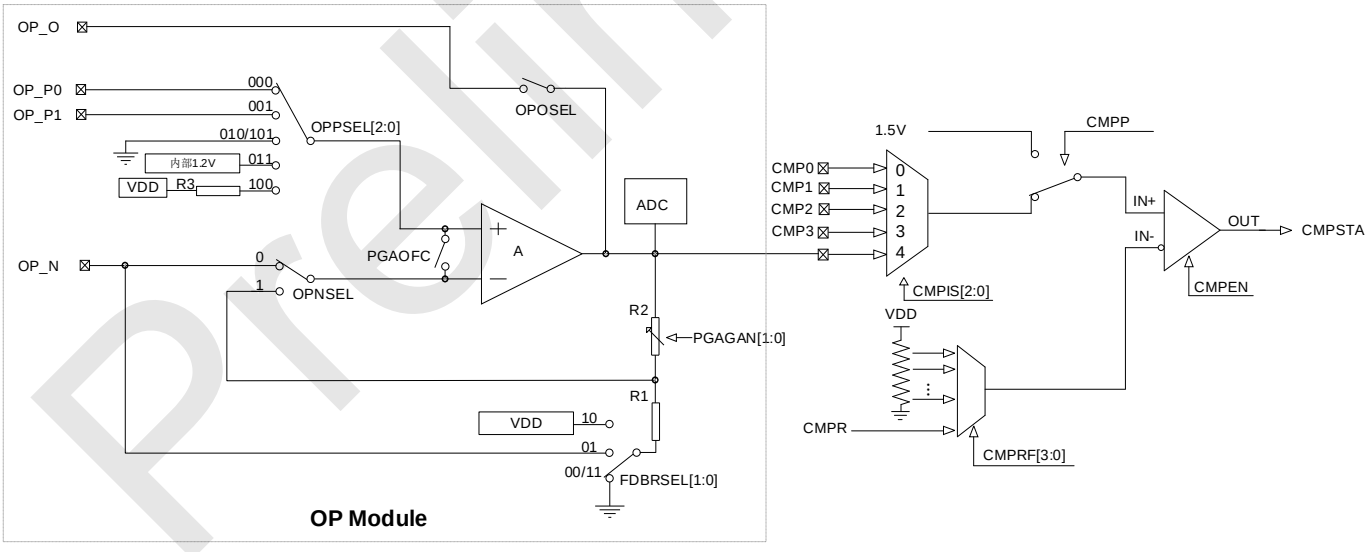
- Positive input of the CMP

When OP is used as the positive input of the CMP, users should set ENOP=1 to enable the OP module, then select OP output port as the CMP input port by channel control bit CMPIS[2:0].

- OP_O pin.

When OP outputs through the OP_O pin,users should set ENOP=1 to enable the OP module,then set OPOSEL=1

11.4 OP Circuit Structure Diagram



OP Module

12 Analog Comparator CMP

12.1 Overview

The SC32F12T/12G series features a built-in analog comparator (CMP), and CMP interrupt can wake up the STOP Mode. It can be used for applications such as alarm circuits, power supply voltage monitoring circuits, zero-crossing detection circuits, etc.

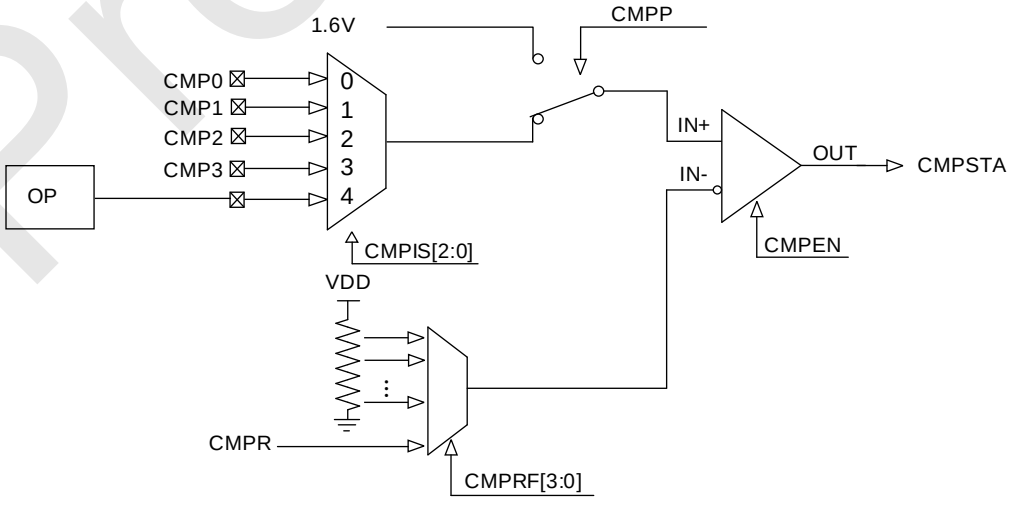
The comparator has five analog signal positive input terminals: CMP0~3 and OP output port, which can be selected through CMPIS [2:0]. The negative input terminal voltage can be switched through CMPRF[3:0] to an external voltage on the CMPR pin or one of the 15 reference voltages internally.

The interrupt mode of the comparator can be conveniently set using CMPIM[1:0]. When the interrupt condition set by CMPIM[1:0] occurs, the comparator interrupt flag CMPIF will set to 1. This interrupt flag needs to be cleared by software.

12.2 Feature

- Positive input has five options:
  - Four analog signal positive input terminals: CMP0~CMP3
  - OP output
- Negative input voltage can be selected from CMPR handover or one of the 15 comparison voltages derived from the internal VDD division
- CMP interrupt can wake up the STOP Mode

12.3 Analog Comparator Structure Diagram



Analog Comparator Structure Diagram

13 UART0~5

13.1 Clock Source

The SC32F12T/12G series UART has only one clock source, which is derived from PCLK

13.2 Feature

- Six UARTs，UART0~5
- UART2 has a complete LIN interface
  - Can switch between master and slave modes
  - Supports hardware break sending in master mode (10/13 bits)
  - Supports hardware break detection in slave mode (10/11 bits)
  - Supports baud rate synchronization in slave mode
  - Provides related interrupts/status bits/flags/fault tolerance range
- UART0~5 support signal port mapping and can be mapped to another set of I/Os
- Each UART has four communication modes to choose from:
  - Mode 0: 8-bit half-duplex synchronous communication mode, serial data is transmitted and received on the RX pin. The TX pin is used as the transmit shift clock. Each frame transmits or receives 8 bits, with the low bit transmitted or received first
  - Mode 1: 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. The communication baud rate is variable
  - Mode 2: Reserved
  - Mode 3: 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, 1 programmable 9th bit and 1 stop bit. The communication baud rate is variable
- Interrupts will be generated and corresponding flags TXIF and RXIF will be set when transmission and reception are complete. Interrupt flags need to be cleared by software
- UART0 and UART1 can generate DMA requests
- UART2~5 cannot generate DMA requests
- Independent baud rate generator
- UART2 does not support waking up from STOP Mode
- UART0/1/3/4/5 support waking up from STOP Mode:
  - The falling edge of the START bit can wake up STOP Mode
  - Provides corresponding wake-up interrupt enable bit WKIE and wake-up interrupt flag WKIF

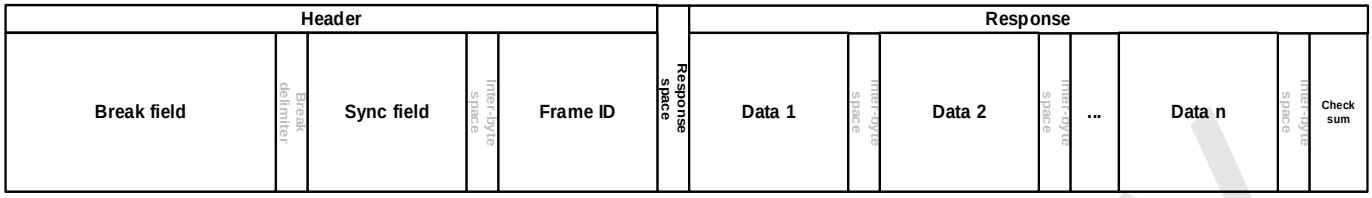
13.3 UART2-LIN

UART2 supports standard LIN communication protocol.

13.3.1 LIN Frame Structure

Under the LIN protocol, all communication information is encapsulated into frames. A frame is composed of a header (provided by the master task) and a response (provided by the slave task). The header (provided

by the master task) consists of a break field, a sync (synchronization) field and a frame ID. The frame ID serves solely to define the purpose of the frame and the slave is responsible for responding to the relevant frame ID. The response consists of a data field and a checksum field.



LIN Frame Structure Diagram

13.3.2 LIN Master Mode

By setting FUNCSEL=1 and SLVEN=0, the UART will support LIN master mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN master mode is as follows:

① Configure the UART_BAUD register to set the baud rate.
② Set FUNCSEL=1 to select the LIN function mode.
③ Set SM[1:0] to 01 to configure the UART in Mode 1.

A complete header consists of a break field, a sync field, and a frame ID. The UART controller can choose the 'break field' as the transmitted header. The 'sync field' and 'frame ID field' need to be written by the user through software, that is to say, to send a complete header to the bus, the software must sequentially fill in the sync data (0x55) and the frame ID data into the UART_DAT register."

13.3.3 LIN Slave Mode

By setting FUNCSEL=1 and SLVEN=1, the UART will support LIN slave mode. In LIN mode, according to the LIN protocol, each byte is initiated with a dominant bit, followed by 8 data bits with no parity bit, LSB first, and ends with a recessive STOP bit.

The initialization process for LIN slave mode is as follows:

① Configure the UART_BAUD register to set the baud rate.
② Set FUNCSEL=1 to select the LIN function mode.
③ Set SM[1:0] to 01 to configure the UART in Mode 1.
④ Set SLVEN to 1 to enable LIN slave mod

In LIN slave mode, the slave break field detection function is enabled by setting LBDL to detect and receive 'break field'. After receiving a break, the BKIF flag will be set and an interrupt will be generated if BKIE is set to 1. To avoid bit rate deviation, users can set SLVAREN to enable automatic resynchronization feature to prevent clock errors.

13.3.4 Synchronization Error Detection

In automatic resynchronization mode, the controller will detect errors in the sync field. The error detection compares the current baud rate with the baud rate of the received sync field, and the following both detections are performed simultaneously.

Check 1: Based on the measurements from the first falling edge to the last falling edge of the sync field,

- If the error exceeds 15%, the header error flag SLVHEIF will be set.
- If the error is between 14% and 15%, the header error flag SLVHEIF may be set (depending on data dephasing).

Check 2: Based on the measurements from each falling edge of the sync field,

- If the error exceeds 19%, the header error flag SLVHEF will be set.
- If the error is between 15% and 19%, the header error flag SLVHEIF may be set (depending on data dephasing).

Note: Error detection is based on the current baud rate clock. Therefore, to ensure the accuracy of error detection, it is recommended that users reload the baud rate to its initial value through software before a new break field is received.

14 SPI0~2

14.1 Clock Source

The SC32F12T/12G series SPI has only one clock source, which is derived from PCLK

14.2 SPI0 Feature

- Supports 11-stage SPI clock pre-scaling
- Signal ports can be mapped to three additional sets of ports
- SPI0 signal ports strong driving
  - In SPI communication mode, the corresponding signal port's pin output driving capability will be enhanced, while in other modes, it remains consistent with the characteristics of a regular I/O.
  - Its mapped signal port can also be set to strong driving to ensure the consistency of SPI0 across any port
- Features a 16-bit 8-level FIFO with independent transmission and reception
  - SPI0's FIFO function allows continuous writing of 8 or fewer 8-bit or 16-bit transmit data to the SPI send buffer (SPI0_DATA). During SPI transmission, the data written into the FIFO first is also sent first. When the data written by the user to the FIFO is sent, the FIFO empty flag TXEIF will be set; if the FIFO is full, the write conflict flag WCOL will be set, and the user cannot write data to the FIFO until the data in the FIFO is sent out and the FIFO is not full. The interrupt flag SPIF will be set only when all the data in the FIFO has been sent
  - Continuously read 8 or fewer 8-bit or 16-bit receive data from the SPI receive buffer (SPI0_DATA), with the first received data being the first to be read
  - FIFO data transfer half-interrupt and corresponding flags for timely reading/writing of data:
    - Provides an interrupt and corresponding flag TXHIF when there is less than half of the valid data in the transmit FIFO
    - Provides an interrupt and corresponding flag RXHIF when there is more than half of the data in the receive FIFO
  - Support recieve buffer overflow interrupt and corresponding flag to promptly notify exceptions
- Support DMA
  - Enable TXDMAEN, and the DMA request can be triggered after the transmit buffer empty flag TXEIF is set.
  - Enable RXDMAEN, and the DMA request can be triggered after the receive buffer not empty status flag RXNEIF is set.

14.3 SPI1/2 Feature

- Supports 11-stage SPI clock pre-scaling
- Signal ports can be mapped to three additional sets of ports
- No FIFO
- Supports DMA
  - SPI1 can generate DMA requests

- SPI2 cannot generate DMA requests

14.4 SPI0 and SPI1/2 Comparison

Comparison / BIT	SPI0	SPI1/2
Signal Port Strong Driving	Available	None
WCOL	When the send FIFO is full, attempting to write to the FIFO will fail, and WCOL will be set, indicating a buffer write conflict	When one frame is sending, attempting to write to the FIFO will fail, and WCOL will be set, indicating a buffer write conflict
SPIF	This position being set indicates the completion of receiving/sending one frame of data	This position being set indicates the completion of receiving/sending one frame of data
RXHIE	Interrupt enable bit for the valid data in the recieve FIFO is more than half	None
TXHIE	Interrupt enable bit for the valid data in the transmit FIFO is less than half	None
RXIE	Interrupt enable bit for the receive FIFO full	None
TBIE	Interrupt enable bit for the transmit FIFO empty	Interrupt enable bit for the transmit FIFO empty
RXNEIE	Interrupt enable bit for the receive FIFO not empty	None
RXHIF	Set when the valid data in the receive FIFO is more than half	None
TXHIF	Set when the valid data in the receive FIFO is less than half	None
RXFIF	Set when the receive FIFO is full	None
TXEIF	Set when the receive FIFO is empty	Set when the receive FIFO is empty
RXNEIF	Recieve FIFO not empty flag	None
DMA	Triggering DMA requests through the TXEIF flag and the RXNEIF flag	SPI1:A request is uniformly set at the end of a frame SPI2:Cannot genarate DMA request

15 TWI0~1

15.1 Clock Source

The SC32F12T/12G series TWI has only one clock source, which is derived from PCLK

15.2 Feature

- Supports 11-stage TWI clock pre-scaling
- Support 2 sets of TWI interfaces: TWI0 and TWI1
- Support TWI signal mapping
  - TWI0 can be mapped to five other groups of IO
  - TWI1 can be mapped to five other groups of IO
- Support master/slave mode
- Bidirectional data transmission between master and slave
- Communication speed can reach up to 1 Mbps
- Support DMA
  - TWI0 can generate DMA requests
  - TWI1 cannot generate DMA requests

15.3 TWI Signal Description

On the TWI bus, data is synchronously transmitted between the master and slave devices using the clock line (SCL) and the data line (SDA). Each data byte has a length of 8 bits, and one data bit is transferred with each SCL clock pulse. The data is transmitted starting from the most significant bit (MSB), and after each byte, an acknowledgment bit follows. Each bit is sampled when SCL is high. Therefore, the SDA line may change when SCL is low, but it must remain stable when SCL is high. When SCL is high, any transition on the SDA line is considered a command (START or STOP)

TWI Clock Signal Line(SCL):

The clock signal is generated by the master and is connected to all the slaves. It transmits one byte of data every 9 clock cycles. The first 8 cycles are used for data transmission, and the last one is used as the acknowledgment clock for receiver. It should be pulled up by the pull-up resistor on the SDA line when idle.

TWI Data Signal Line(SDA)

SDA is a bidirectional signal line and should be pulled up by the pull-up resistor on the SDA line when idle.

16 Hardware Watchdog WDT

The SC32F12T/12G series features a built-in hardware watchdog (WDT) with an internal 32kHz oscillator as its clock source. Users can choose to enable the watchdog reset function by setting the ENWDT control bit in the Code Option through a programmer.

The hardware watchdog timer (WDT) is known for its high safety, accurate timing, and flexible usage. This watchdog peripheral can detect and resolve faults caused by software errors, and it will trigger a system reset when the counter reaches overflow time.

The WDT is driven by its internal low-frequency oscillator, which allows it to remain operational even if the main clock fails.

16.1 Clock Source

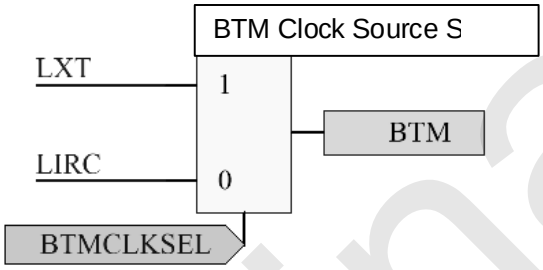
The SC32F12T/12G series WDT is fixed to LIRC. Once the WDT is enabled, LIRC will automatically start, and it will remain oscillating throughout the operation of the WDT and users cannot turn off LIRC while the WDT is active.

17 Base Timer（BTM）

The SC32F12T/12G series features a Base Timer (BTM) that can generate interrupts at intervals ranging from 15.625ms to 32s. The BTM can use either 32kHz LIRC or external 32.768kHz crystal oscillator (LXT) as its clock source. The interrupts generated by the BTM can wake up the CPU from STOP mode.

17.1 Clock Sourse

SC32F12T/12G series BTM can choose LXT or LIRC as its clock sourse



17.2 Feature

- Selectable interrupt frequency intervals from 15.625ms to 32s
- Can wake up from STOP Mode

18 Built-in CRC Module

The SC32F12T/12G series has a built-in CRC (Cyclic Redundancy Check) module that utilizes a polynomial generator to generate CRC codes from an 8-bit/16-bit/32-bit data word.

18.1 Clock Source

The SC32F12T/12G series CRC has only one clock source, which is derived from HCLK.

18.2 Feature

- 1 built-in hardware CRC module
- Configurable initial value, with a default of 0xFFFF_FFFF
- Supports 8-bit/16-bit/32-bit data units
- Programmable polynomial, with a default of 0x04C1_1DB7
- Only supports software-driven data computation mode
- Supports DMA: CRC_DR can serve as the DMA destination address or be accessed directly via registers
- Calculating CRC for a single byte requires 1 system clock

CRC algorithm	CRC-32/MPEG-2
Polynomial Formula	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$
Data Width	32bit
Inital Value	0xFFFF_FFFF
Result XOR Value	0x0000_0000
Input Value Reversal	false
Output Value Reversal	false
LSB/MSB	MSB

Note: The written and read data in CRCDR cannot be the same.

19 PWM0: 8 Channels of 16-bit Multifunctional PWM

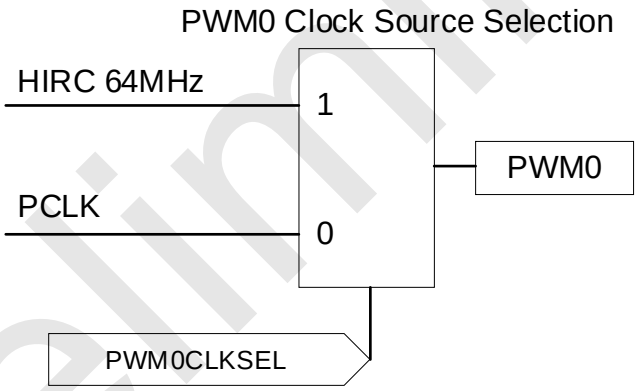
19.1 Overview

The PWM0 of the SC32F12T/12G series is an 8-channel 16-bit shared-cycle multifunctional PWM. PWM0 has rich functionalities, including support for adjusting the cycle and duty cycle, the option to choose between center-aligned or edge-aligned output waveforms, selectable independent or complementary output modes, support for dead-time functionality, and a fault detection mechanism. The Register PWM0_CON and PWM0_STS control the state and cycle of the PWM. Each channel of PWM can be individually adjusted for enabling, output waveform, waveform inversion, and duty cycle.

19.2 Clock Source

The SC32F12T/12G series PWM0 can choose HIRC or PCLK as its clock source

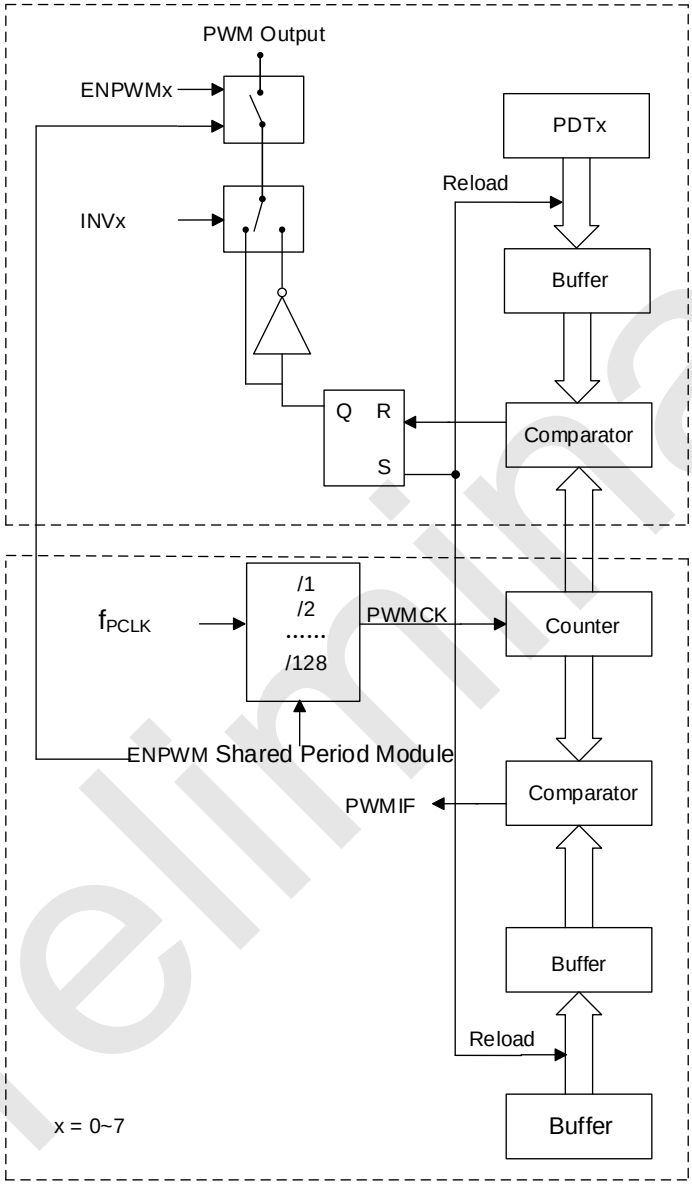
- PWM0 output frequency is at its maximum the frequency of the selected clock source
- PWM0 clock pre-scaler can select from 1 to 128



19.3 Feature

- 8 channels of 16-bit shared-period multifunctional PWM
- The output waveform can be inverted
- Waveform types: can be set as center-aligned or edge-aligned
- PWM modes: can be set as independent mode or complementary mode:
  - In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
  - In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously
- Provides one PWM overflow interrupt
- Supports fault detection
- Has independent interrupt request flags

19.4 PWM0 Structure Diagram



PWM0 Structure Diagram

19.5 PWM0 General Configuration

19.5.1 Output Mode

- In independent mode, all 8 PWM channels share the same period, but the duty cycle of each PWM channel can be adjusted independently
- In complementary mode, four pairs of complementary PWM waveforms with dead time can be generated simultaneously

19.5.2 Alignment Type

- Edge-aligned
- Center-aligned

19.5.3 Duty Cycle Change Characteristics

When generating the PWM0n output waveform, if it is necessary to change the duty cycle, it can be achieved by modifying the high-level setting register (PDT0x). However, it is important to note that changing the value of PDT0x will not immediately alter the duty cycle. Instead, the change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.

19.5.4 Period Change Characteristics

When generating PWM output waveforms, if it is necessary to change the period, it can be achieved by modifying the period setting register PWMPD. Similar to the duty cycle, changing the value of PWMPD will not immediately alter the period. The change takes place when the PWM counter counts to 0 or counts up to a value matching the setting in the period setting item PWMPD[15:0] +1.

20 LEDPWM: 8 Channels of 32-bit LEDPWM

20.1 Clock Source

The SC32F12T/12G series LEDPWM has only one clock source, which is derived from PCLK2.

20.2 Feature

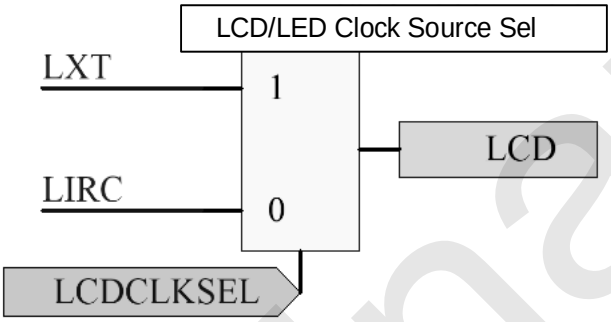
- Shared period and independently adjustable duty cycle
- Support center-aligned mode for driving LEDs conveniently
- Duty cycle register shares with 28 SEG registers, serving as an alternative to LED circuits, generating LED driving waveforms
- The highest pre-scaling option is /256, with each step being 2^n
- Support independent interrupt request flags
- Achieve grayscale adjustment through center-aligned LEDPWM：
  - In grayscale adjustment, one COM corresponds to a maximum of 28 duty values, offering options like 8 X 24, 6 X 26, 5 X 27, 4 X 28
  - During LEDPWM interrupts, switch COM and write corresponding duty value into DUTY register of LEDPWM can achieve the adjustment of each SEG's grayscale.

21 LCD/LED Driver

LCD/LED option, sharing registers and I/O ports

21.1 Clock Source

SC32F12T/12G series LCD/LED can choose LXT or LIRC as its clock sourse



21.2 Built-in 8 COM x 24 SEG LED Driver

- 1/1~1/8 duty voltage driving mode
- LED segment source driving capability with four-level control
- Support common cathode mode/common anode mode swithing through software
- Gray scale adjustment can be achieved by center-aligned PWM: by using 32-channel PWM, with each PWM has its own period buffer and duty buffer

21.3 Built-in 8 COM x 24 SEG LCD Driver

- Type A / Type B waveform selectable
- 8 X 24、6 X 26、5 X 27、4 X 28
- Optional voltage division resistor for LCD voltage output port
- LCD display driver bias voltage
  - 1/4 bias voltage
  - 1/3 bias voltage
- Three selectable frame rates:
  - Type A mode 32/64/128Hz
  - Type B mode 64/128/256Hz

22 39-Channel High-Sensitivity Touch Key Circuit(TK)

- High-sensitivity mode
- Suitable for touch applications with high sensitivity requirements, such as proximity sensing and touch keys
- Channels can be scanned in parallel
- The CMOD capacitor can only be externally connected
- Support self-capacitance mode and mutual-capacitance mode
- Support low-power mode
- Support fast wake-up STOP Mode
- Comprehensive development support: Highly flexible touch software library, intelligent debugging software

Note: Exclusive to the SC32F12T series

23 16-bit Timers (Timer0~Timer7)

23.1 Clock Source

- In timer mode/PWM output mode, the TIM clock source is derived from PCLK
- In counter mode, the Tn pin serves as the counting source input

23.2 Feature

- Supports 8-stage TIM clock pre-scaling
- 8 independent 16-bit auto-reload counters: Timer0 to Timer7
- 16-bit incremental, decremental, and increment/decrement auto-reload counters
- Support rising/falling edge capture, enabling PWM duty and period capture
- Overflow and capture events of TIM1/2/6 can generate DMA requests

23.3 Counting method

23.3.1 Counting Method in Timer Mode

- Upward Counting: Counts from the set value upwards to overflow at 0xFFFF
- Downward Counting: Counts from 0xFFFF downwards to the set value

23.3.2 Counting Method in PWM Mode

Only upward counting mode is available in PWM output mode: The counter starts from 0 and counts up until PDT, then PWM output waveform will switch between the high and low levels. The counting will then continue up to RLD, causing an overflow and the counter reset to 0.

The formula of TPWM is shown as follows:

$$T_{PWM} = \frac{RLD[15:0] + 1}{PCLK}$$

The formula of duty is shown as follows:

$$duty = \frac{PDT[15:0]}{RLD[15:0] + 1}$$

23.4 Timer Signal Port

- Tn, n=0~7
  - Clock input/output
  - Both rising and falling edges can be captured
- TnEX, n=0~7
  - In reload mode, the external event input (falling edge) on the TnEX pin is used for reload enable/disable control

- In capture mode, when FSEL = 1, it serves as a falling edge capture signal input. Detection of a falling edge on the TnEX pin generates a capture, sets EXIF, and captures the value of the TnCNT register into the FCAP register

- TnPWM, n=0~7
  - TIM0~7 can provide PWM with independently adjustable duty cycle through the Tn port: TnPWMA
  - TIM0~7 can provide PWM with independently adjustable duty cycle through the TnEX port: TnPWMB
  - Optional clock source follows TIM
  - Note: TIM's PWM capture function and PWM output function cannot be enabled simultaneously

23.5 Interrupts and Corresponding Flags for TIM

- Overflow/underflow of the counter share the interrupt flag TIF
- Capture status flags:
  - EXIF: Flag indicating detection of a falling edge on the external event input
  - EXIR: Flag indicating detection of a rising edge on the external event input
- Interrupt and priority configuration control bits are merged into the NVIC module

24 Direct Memory Access (DMA)

24.1 Overview

The DMA controller is designed for high-speed data transfer, allowing the movement of data from one address to another without the need for CPU intervention. Leveraging DMA for data transfer can reduce the workload on the CPU, enabling the saved CPU resources to be utilized for other applications. The DMA controller comprises 2 channels, each directly connected to dedicated hardware DMA requests. Additionally, each channel supports software triggering. The DMA controller features support for 4-level channel priority, facilitating the management of priority between DMA requests to ensure that only one DMA channel operates at any given time. It also supports both single and batch transfers, with the request source being either a software request or an interface request. Data transfer between memories is accomplished using software requests.

Note: For a bidirectional data transfer application, two DMA channels are required to handle sending and receiving operations.

24.2 Clock Source

The clock source of DMA is derived from HCLK, and the external peripheral clock of DMA is enabled through AHB_CFG.DMAEN.

24.3 Feature

- Support 2 independent configurable channels
- Support 4 priority levels for requests
- Support 8-bit, 16-bit, 32-bit data transfers
- Support automatic increment or fixed source and destination addresses, with data widths of byte, half-word, and word
- Support single and burst transfer modes

24.4 Function Description

24.4.1 Transmission

No transmit limitation between peripheral and memory for DMA：

Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory	Peripheral-to-Periphral
No limitation	No limitation	No limitation	No limitation

24.4.2 DMA Access Restriction

Users are not allowed to perform write operations on Flash or access the core through DMA. Violating these restrictions may lead to unpredictable exceptions.

24.4.3 Channel Priority

There are 4 priority levels can be configured through PL[1:0] registers:

- 00: Low
- 01: Medium
- 10: High
- 11: Very High

24.4.4 Single Transmission and Burst Transmission

The DMA controller supports single and burst data transfer types, and the request source can be a software request or an interface request while data transfer between memory is done by software requests. Single transfer means that the software or interface is ready to transfer one data (each data requires one request), while burst transfer means that the software or interface will transfer multiple data (multiple data requiring only one request).

The modes of single and burst transfer can be set through TPTYPE register (DMAn_CFG[15]).

In single transfer mode, each transfer of data requires one request. As each data is transferred, the values in the register DMAn_CNT[31:0](n=0~3) decrease by 1, the transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0. In this mode, BURSIZE (DMAn_CFG[14:12]) is not used to control the size of the transferred data and its value is fixed at 1.

In burst transfer mode, DMA transfer DMAn_CNT[31:0] data with only one request. After transferring BURSIZE (DMAn_CFG[14:12]) data, the value in DMAn_CNT[31:0] is decreased by BURSIZE. The transfer of data is completed when the count in DMAn_CNT[31:0] becomes 0.

24.4.5 Loop Mode

The loop mode can be used to handle circular buffers and continuous data streams (such as ADC scan mode). During the loop mode transfer, the number of data to be transferred will automatically reload to the initial value set in the channel configuration phase and continue to respond to DMA requests. To stop loop transfer, the software needs to stop the generation of DMA requests by the peripheral before disabling the DMA channel (for example, exiting ADC scan mode). The software must explicitly set the DMACNT value before starting/enabling the transfer and after stopping the loop transfer.

The SC32F12T/12G series DMA controller supports normal mode and loop mode:

- When CIRC=0 (DMA channel is in non-loop mode), it will no longer accept any DMA requests after reaching the set number of data to be transferred
- When CIRC=1 (DMA channel is in loop mode), after the transfer is complete, the DMACNT of the channel will automatically reload the previously set value and wait for the next loop

Users can flexibly choose according to their actual needs.

25 SysTick

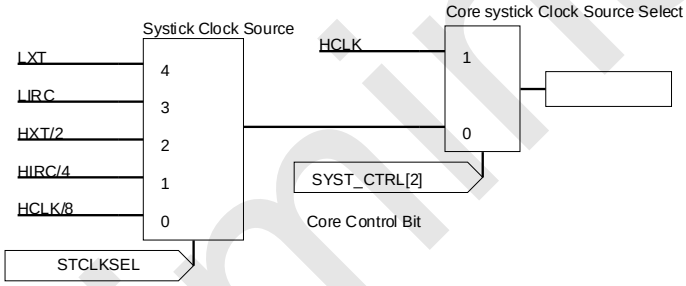
SysTick is a simple, 24-bit, writable-clear, decrementing automatic reload counter with a flexible control mechanism. This counter can be used as a tick timer for a Real-Time Operating System (RTOS) or as a simple counter.

25.1 Clock Source

SysTick (Cortex®-M0+ Core System Timer) has internal clock source and external clock source：

- Internal clock source: CPU Clock
- 5 external clock sources

SysTick clock sourse diagram is as follow:



25.2 SysTick Calibration Register Default Value

The calibration value for the SysTick Calibration Register is set as follows:

- If the default clock after power-on is f_{HCLK}/n (MHz), where n is the default power-on divider, and the default clock source is HIRC
- Then, setting the initial SysTick calibration value to 1000 * (f_{HCLK}/n) will generate a 1ms time reference

26 Electrical Characteristics

Unless otherwise specified, the electrical data in this section are based on the working conditions listed in the “Recommended Operating Conditions” subsection.

26.1 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	Operating voltage	2.0	5.5	V	f_{HCLK}=64MHz Clock source is HIRC
T_A	Ambient temperature	-40	105	℃	

26.2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	6	V
V_{PIN}	Input/output voltage of any pin	-0.3	V_{DD}+0.3	V
T_A	Ambient temperature	-40	105	℃
T_{STG}	Storage temperature	-55	125	℃
I_{VDD}	Current value flowing through VDD	-	200	mA
I_{VSS}	Current value flowing through VSS	-	200	mA

26.3 Flash ROM Parameters

VDD = 5V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
N_{END}	Endurance earse/write cycles	100,000	-	-	Cycles	Clock source is HIRC
T_{DR}	Data retention time	100	-	-	Years	
$T_{S\text{-}Erase}$	Single sector erase time	-	5	-	ms	
T_{Erase}	Page erase time	30	-	40	ms	
T_{Write}	Single byte write time	-	34	-	μs	

Note: IAP (In-Application Programming) must be aligned by word when writing, therefore the write time for a single byte is the same as for a single word.

26.4 Power Consumption

26.4.1 VDD = 5V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Boot Area	Min	Typical	Max	Unit	Conditions
I_{op1}	Operating current	APROM	-	7	-	mA	f_{HCLK}=64MHz Clock source is HIRC
			-	4.2	-	mA	f_{HCLK} =32MHz Clock source is HIRC
			-	2.7	-	mA	f_{HCLK} =16MHz Clock source is HIRC
			-	2	-	mA	f_{HCLK} =8MHz Clock source is HIRC
			-	1.6	-	mA	f_{HCLK} =4MHz Clock source is HIRC
I_{pd1}	Power Down Mode current	APROM	-	3.0	-	μA	f_{HCLK} =64MHz Clock source is HIRC
I_{IDL1}	IDLE Mode current	APROM	-	1.8	-	mA	f_{HCLK} =64MHz Clock source is HIRC

26.4.2 VDD = 3.3V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Boot Area	Min	Typical	Max	Unit	Conditions
I_{op2}	Operating current	APROM	-	7	-	mA	f_{HCLK}=64MHz Clock source is HIRC
			-	4.2	-	mA	f_{HCLK} =32MHz Clock source is HIRC
			-	2.7	-	mA	f_{HCLK} =16MHz Clock source is HIRC
			-	2	-	mA	f_{HCLK} =8MHz Clock source is HIRC
			-	1.6	-	mA	f_{HCLK} =4MHz Clock source is HIRC
I_{pd2}	Power down Mode current	APROM	-	2.1	-	μA	f_{HCLK} =64MHz Clock source is HIRC
I_{IDL2}	IDLE Mode current	APROM	-	1.8	-	mA	f_{HCLK} =64MHz Clock source is HIRC

26.5 GPIO Parameter

26.5.1 VDD = 5V,TA = +25℃,unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH1}	Input high voltage	$0.7V_{DD}$	-	V_{DD}+0.3	V	
V_{IL1}	Input low voltage	-0.3	-	$0.3V_{DD}$	V	
V_{IH2}	Schmitt trigger input high voltage	$0.8V_{DD}$	-	V_{DD}	V	Schmitt trigger input: NRST T_CLK / T_DIO UART0~5 enter RX SPI / TWI signal input INT0~INT15 PWM fault detection port FLT Timer clock input Tn Timer capture port TnEX
V_{IL2}	Schmitt trigger input low voltage	-0.2	-	$0.2V_{DD}$	V	
I_{OL1}	Regular driving IO ports Output low current	-	27	-	mA	V_{Pin}=0.4V
I_{OL2}	Regular driving IO ports Output low current	-	50	-	mA	V_{Pin}=0.8V
$I_{OHSPI0A}$	SPI0 signal port: MISO0 MOSI0 SCK0 Output high current @V_{Pin}=4.3V	-	24	-	mA	Transferring data through SPI0
$I_{OHSPI0B}$	SPI0 signal port: MISO0 MOSI0 SCK0 Output high current @V_{Pin}=4.7V	-	11	-	mA	Transferring data through SPI0
I_{OH1}	Output high current @ V_{Pin}=4.3V	-	12	-	mA	Pxyz=0,I_{OH} level 0
		-	9	-	mA	Pxyz=1,I_{OH} level 1
		-	6	-	mA	Pxyz=2,I_{OH} level 2
		-	3	-	mA	Pxyz=3,I_{OH} level 3
I_{OH2}	Output high current @ V_{Pin}=4.7V	-	5	-	mA	Pxyz=0,I_{OH} level 0
		-	4	-	mA	Pxyz=1,I_{OH} level 1

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
		-	2.8	-	mA	Pxyz=2,I_{OH} level 2
		-	1.4	-	mA	Pxyz=3,I_{OH} level 3
I_{lkg1}	Input leakage current	-1	-	1	μA	IO is in high-impedance input mode V_{IN}=V_{DD} or V_{SS}
R_{PH1}	Pull-up resistance	15	30	45	kΩ	V_{IN}=V_{SS}

26.5.2 VDD = 3.3V,TA = +25℃, unless otherwise specified

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IH3}	Input high voltage	0.7V_{DD}	-	V_{DD}+0.3	V	
V_{IL3}	Input low voltage	-0.3	-	0.3V_{DD}	V	
V_{IH4}	Input high voltage	0.8V_{DD}	-	V_{DD}	V	Schmitt trigger input: NRST T_CLK / T_DIO UART0~5 enter RX SPI / TWI signal input INT0~INT15 PWM fault detection port FLT Timer clock input Tn Timer capture port TnEX
V_{IL4}	Input low voltage	-0.2	-	0.2V_{DD}	V	
I_{OL3}	Regular driving IO ports Output low current	-	20	-	mA	V_{Pin}=0.4V
I_{OL4}	Regular driving IO ports Output low current	-	35	-	mA	V_{Pin}=0.8V
$I_{OHSPI0C}$	SPI0 signal port: MISO0 MOSI0 SCK0 Output high current @V_{Pin}=3.0V	-	9	-	mA	Transferring data through SPI0
I_{OH3}	Output high current @ V_{Pin}=3.0V	-	3.7	-	mA	Pxyz=0,I_{OH} level 0
		-	3	-	mA	Pxyz=1,I_{OH} level 1
		-	2	-	mA	Pxyz=2,I_{OH} level 2
		-	1	-	mA	Pxyz=3,I_{OH} level 3
I_{lkg2}	Input leakage current	-1	-	1	μA	IO is in high-impedance input mode V_{IN}=V_{DD} or V_{SS}

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
R_{PH2}	Pull-up resistance	25	50	75	kΩ	$V_{IN}=V_{SS}$

26.6 TK Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{TK}	High sensitivity Touch key working current @5V	-	0.8	1.2	mA	f_{HCLK}=64MHz
	High sensitivity Touch key working current @3.3V	-	0.7	1.0	mA	f_{HCLK}=64MHz

26.7 BTM Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{BTM}	Base Timer working current @5V	-	1.3	3	μA	BTMCLKSEL=0 Clock source is LIRC
	Base Timer working current @3.3V	-	1.2	3	μA	BTMCLKSEL=0 Clock source is LIRC

26.8 WDT Characteristics

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{WDT}	WDT working current @5V	-	1.3	3	μA	
	WDT working current @3.3V	-	1.2	3	μA	

26.9 AC Electrical Characteristics

(V_{DD} = 2.0V ~ 5.5V,T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
T_{LXT}	External 32kHz oscillator start-up time	-	1	-	s	External 32kHz crystal oscillator
T_{POR}	Power On Reset time	-	15	-	ms	
T_{PDW}	Power Down Mode wake-up time	-	65	130	μs	
T_{Reset}	Reset pulse width	18	-	-	μs	low-level active
T_{LVR}	LVR debounce time	-	30	-	μs	
f_{HIRC}	HIRC oscillator stability	63.36	64	64.64	MHz	V_{DD}=2.0~5.5V T_A=-40~105 ℃
f_{LIRC}	LIRC oscillator stability	30.72	32	33.28	KHz	V_{DD}=4.0~5.5V T_A=-20~85 ℃

26.10 ADC Characteristics

(T_A = 25℃,unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{ADC}	Supply Voltage	2.7	5.0	5.5	V	Vref = 2.048V
		2.0	5.0	5.5	V	Vref = 1.024V or Vref = V_{DD}
		2.7	5.0	5.5	V	Vref = 2.4V
V_{REF1}	Internal reference 2.048V	2.033	2.048	2.063	V	V_{DD} = 2.7~5.5V
V_{REF2}	Internal reference 1.024V	1.004	1.024	1.044	V	V_{DD} = 2.0~5.5V
V_{REF3}	Internal reference 2.4V	2.37	2.40	2.45	V	V_{DD} = 2.7~5.5V
N_R	Precision	-	14	-	bit	GND≤V_{AIN}≤V_{DD}
V_{AIN}	ADC Input voltage	GND	-	V_{DD}	V	
R_{AIN}	ADC Input resistance	1	-	-	MΩ	V_{IN}=5V
I_{lkg_ADC}	ADC Input leakage current	-1		1	μA	V_{IN}= V_{AINx}
I_{ADC}	ADC conversoin current	-	-	2	mA	ADC Module on V_{DD}=5V
		-	-	1.8	mA	ADC Module on V_{DD}=3.3V
DNL	Differential nonlinear error	-	-	±19	LSB	V_{DD}=5V V_{REF}=5V
INL	Integral nonlinear error	-	-	±16	LSB	
E_Z	Offset error	-	-	±20	LSB	
E_F	Full scale error	-	-	±15	LSB	
E_{AD}	Total absolute error	-	-	±20	LSB	
T_{ADC}	ADC conversion time	-	1.1	1.4	μs	LOWSP[2:0] = 100 f_{HCLK} =32MHz, Clock source is HIRC
		-	1.2	1.5	μs	LOWSP[2:0] = 101 f_{HCLK} =32MHz, Clock source is HIRC
		-	1.5	1.9	μs	LOWSP[2:0] = 110 f_{HCLK} =32MHz, Clock source is HIRC
		-	2.0	2.6	μs	LOWSP[2:0] = 111 f_{HCLK} =32MHz, Clock source is HIRC

26.11 CMP Electrical Characteristics

(V_{DD} =5V,T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
V_{CM}	Input voltage range	0	-	V_{DD}	V	
V_{OS}	Offset voltage	-	10	30	mV	
V_{HYS}	comparator voltage hysteresis	-	40	-	mV	
I_{CMP}	Comparator switching current	-	-	100	μA	V_{DD}=5V
T_{CMP}	Response time	-	-	2	μs	

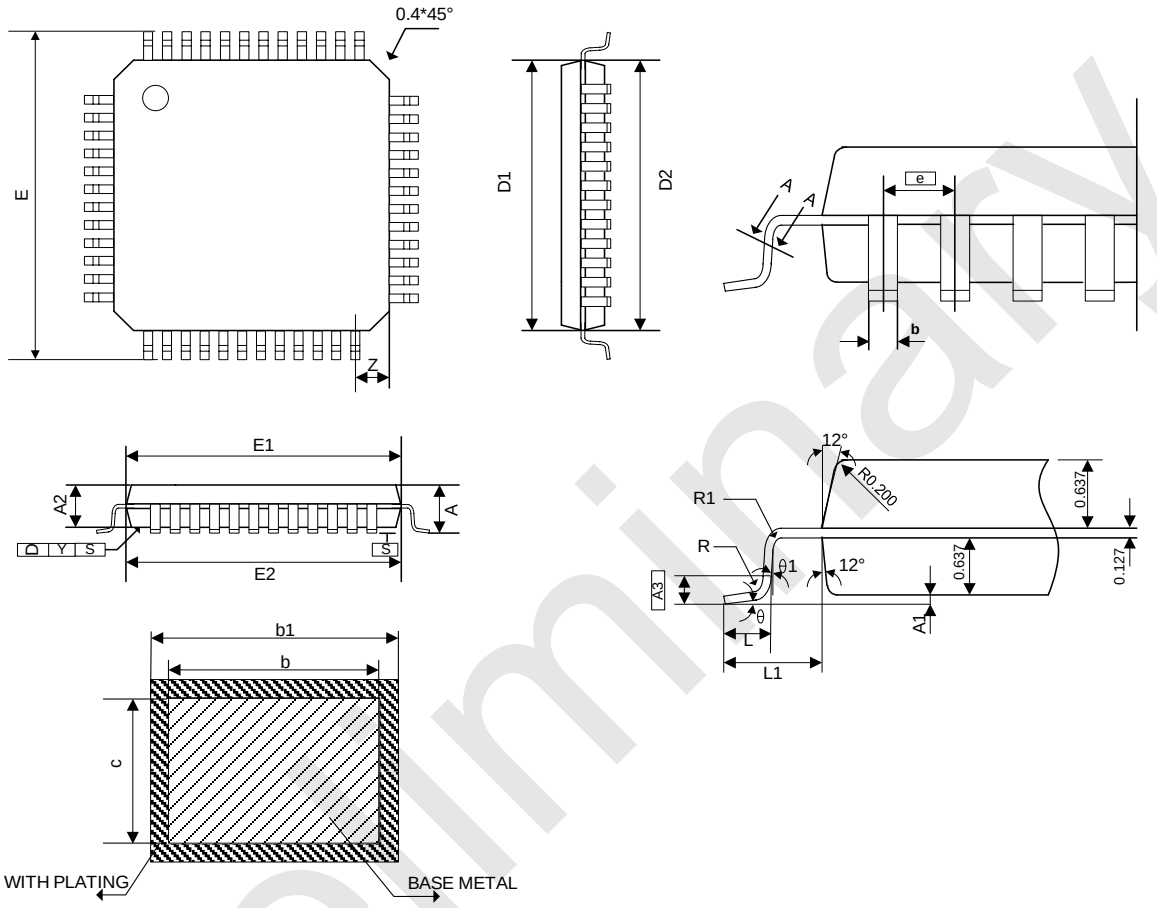
26.12 OP Electrical Characteristic

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
I_{OP}	OP working current	-	1	1.3	mA	
V_{OPO}	OP output voltage	0	-	5.1	V	
G_{PGA}	PGA non-inverting gain	7	8	9		Non-inverting gain = 8
		15	16	17		Non-inverting gain = 16
		30	32	34		Non-inverting gain = 32
		60	64	68		Non-inverting gain = 64
	PGA inverting gain	6	7	8		Inverting gain = 7
		14	15	16		Inverting gain = 15
		29	31	33		Inverting gain = 31
		59	63	67		Inverting gain = 63
R_{PGA}	PGA non-inverting R2/R1 internal resistance value	-	70/10	-	kΩ/ kΩ	Non-inverting gain = 8
		-	150/10	-	kΩ/ kΩ	Non-inverting gain = 16
		-	310/10	-	kΩ/ kΩ	Non-inverting gain = 32
		-	630/10	-	kΩ/ kΩ	Non-inverting gain = 64
	PGA inverting R2/R1 internal resistance value	-	70/10	-	kΩ/ kΩ	Inverting gain = 7
		-	150/10	-	kΩ/ kΩ	Inverting gain = 15
		-	310/10	-	kΩ/ kΩ	Inverting gain = 31
		-	630/10	-	kΩ/ kΩ	Inverting gain = 63

Symbol	Parameter	Min	Typical	Max	Uint	Conditions
RΔ	R1/R2 resistance variation	-20	-	+20	%	

27 Package information

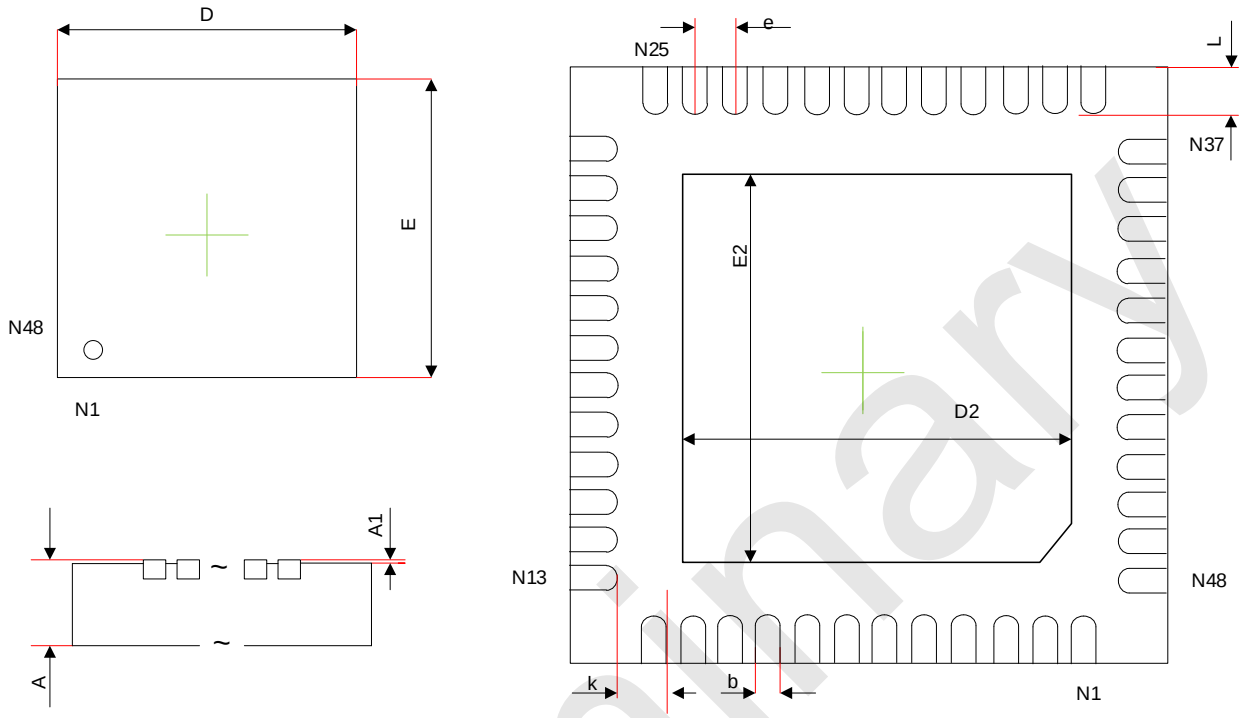
LQFP48 (7X7) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.15	0.20	0.25
b1	0.16	0.22	0.28
c	0.12	--	0.17
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.8	9.00	9.20

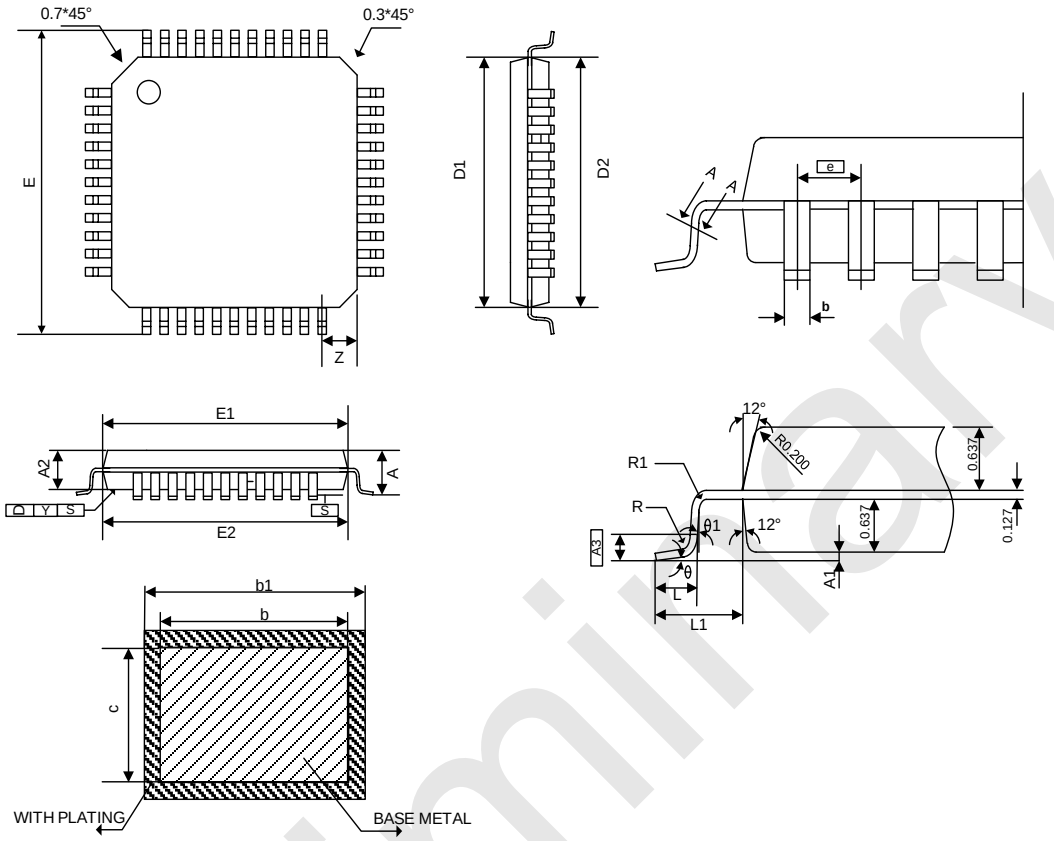
Symbol	mm(milimetre)		
	Min	Normal	Max
E1	6.85	6.95	7.05
E2	6.9	7.00	7.10
e	--	0.5	--
L	0.43	--	0.75
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.75	--

QFN48 (5X5) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.12	--	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35 BSC.		
k	0.20	0.30	--
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40

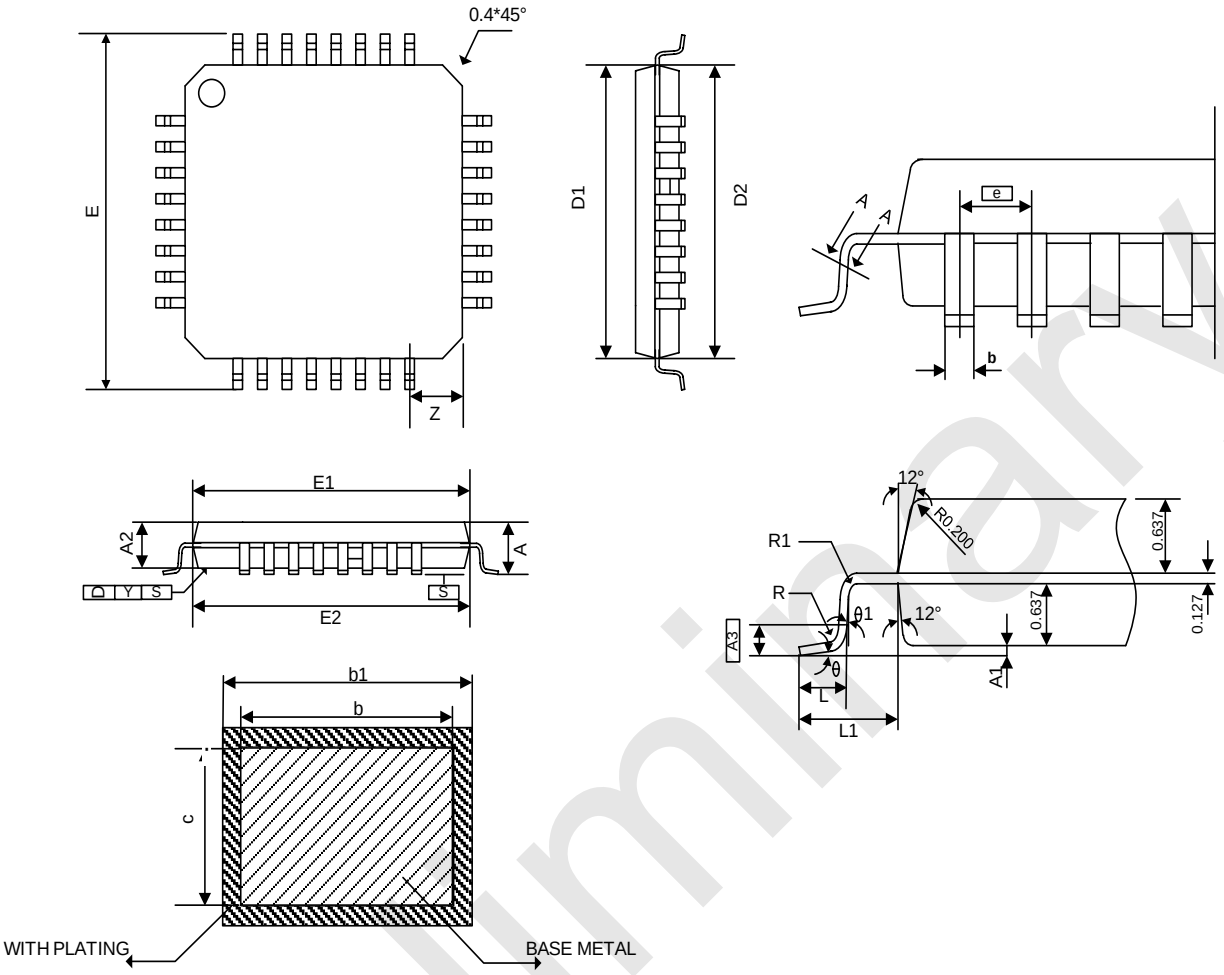
LQFP44 (10X10) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.015	--	0.21
A2	1.3	1.4	1.5
A3	--	0.254	--
b	0.25	0.30	0.36
b1	0.26	0.32	0.38
c	0.12	0.13	0.14
D1	9.85	9.95	10.05
D2	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.85	9.95	10.05
E2	9.90	10.00	10.10
e	--	0.8	--
L	0.42	--	0.75
L1	0.95	1.0	1.15

Symbol	mm(milimetre)		
	Min	Normal	Max
R	0.08	--	0.25
R1	0.08	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	1.0	--

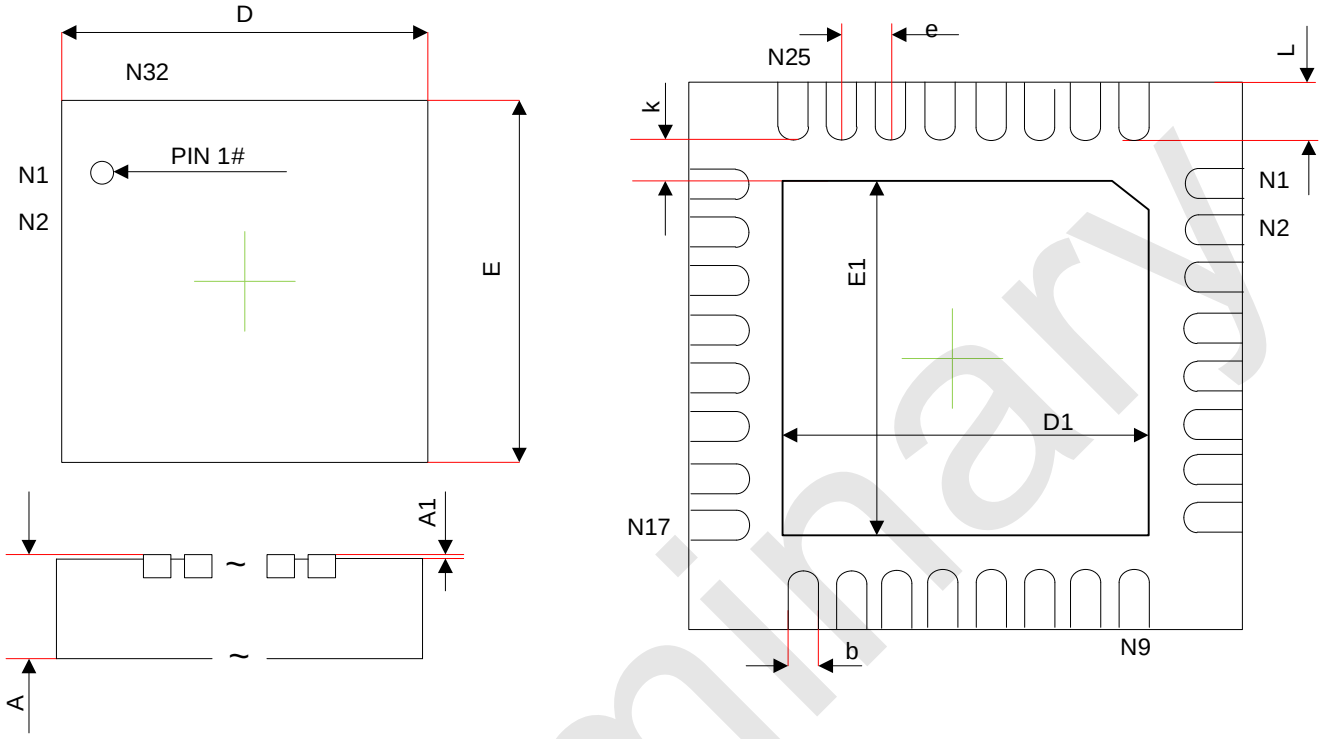
LQFP32 (7X7) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	1.45	1.55	1.65
A1	0.01	--	0.21
A2	1.30	1.4	1.5
A3	--	0.254	--
b	0.30	0.35	0.41
b1	0.31	0.37	0.43
c	0.12	0.13	0.14
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10

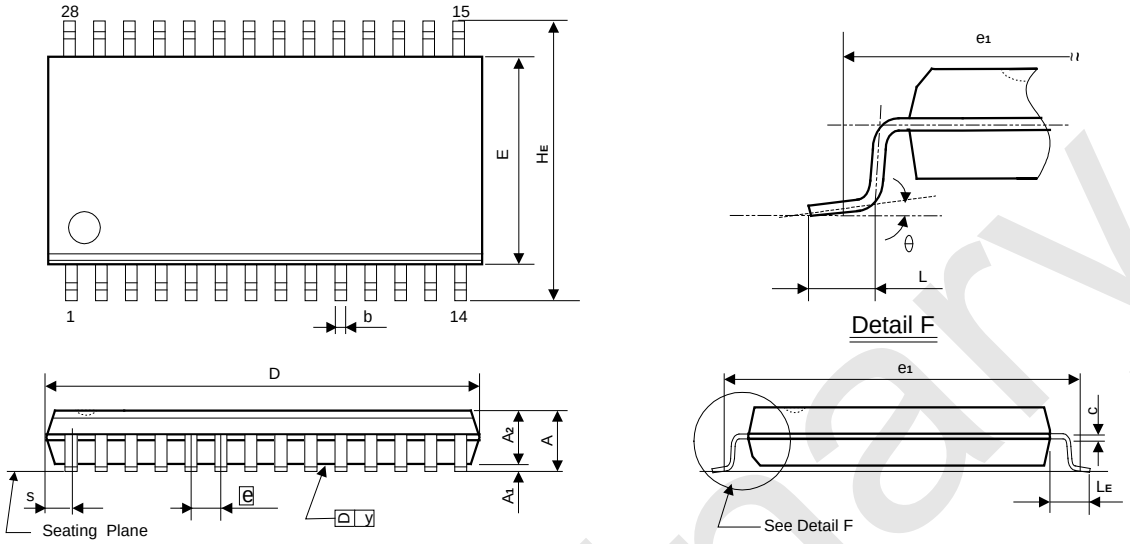
Symbol	mm(milimetre)		
	Min	Normal	Max
e	--	0.8	--
L	0.43	--	0.75
L1	0.90	1.0	1.10
R	0.1	--	0.25
R1	0.1	--	--
θ	0°	--	10°
θ1	0°	--	--
y	--	--	0.1
Z	--	0.70	--

QFN32 (4X4) Dimension (Unit: mm)



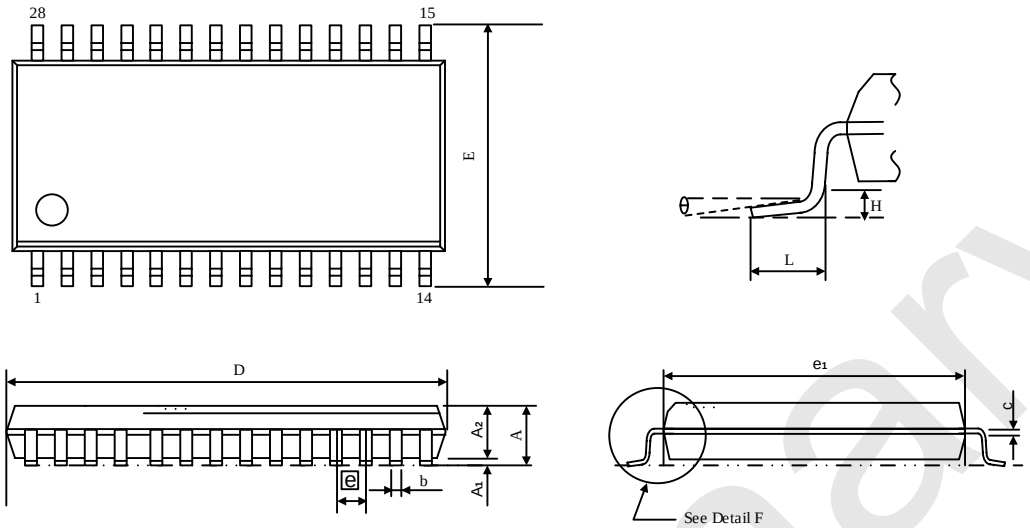
Symbol	mm(milimetre)		
	Min	Normal	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40 BSC		
k	0.2	--	--
D1	2.60	--	2.90
E1	2.60	--	2.90
L	0.22	--	0.45

SOP28L(300mil) Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	2.40	2.56	2.65
A1	0.100	0.200	0.300
A2	2.240	2.340	2.440
b	0.39	---	0.48
C	0.254(BSC)		
D	17.80	18.00	18.20
E	7.30	7.50	7.70
HE	10.100	10.300	10.500
e	1.270(BSC)		
L	0.7	0.85	1.0
LE	1.3	1.4	1.5
θ	0°	-	8°

TSSOP28L Dimension (Unit: mm)



Symbol	mm(milimetre)		
	Min	Normal	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	9.600	-	9.800
E	6.250	-	6.550
e1	4.300	-	4.500
e	0.65(BSC)		
L	-	-	1.0
θ	0°	-	8°
H	0.05	-	0.25

28 Revision History

Version	Notes	Date
V0.1	Initial Release	2024.04.23

29 Important Notice

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